Design Framework for Soft-Error-Resilient Sequential Cells

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***Abstract*—This paper presents a design framework for soft-error-resilient sequential cells, by introducing a new sequential cell called LEAP-DICE and evaluating it against existing circuit techniques in the "soft error resilience-power-delay-area" design space in an 180 nm CMOS test chip. LEAP-DICE, which employs both circuit and layout techniques, achieved the best soft error performance with a 2,000X improvement over the reference D flip-flop with moderate design costs. This study also discovered new soft error effects related to operating conditions.**

***Index Terms*—CMOS integrated circuits, DICE, LEAP, radiation hardening, sequential circuits, soft error.**

I. Introduction

SOFT errors pose a major reliability concern for robust computer systems [1]. Sequential elements, such as flip-flops and latches, cannot be protected using efficient word-level techniques such as error correcting codes that are applicable to large SRAM arrays. Therefore, the design of new *soft-error-resilient* sequential elements is important. With technology scaling, the distance between sensitive circuit nodes decreases, and the probability of *Single-Event Multiple Upsets* (SEMU), also called *Multiple-Bit Upset* (MBU), where a single particle strike simultaneously upsets multiple circuit nodes, increases significantly [2]. SEMUs cannot be protected using standard hardness-by-design circuit techniques. This paper addresses those concerns through the design of soft-error-resilient flip-flops using a combination of circuit and layout techniques.

The major contributions of this paper are as follows:

1) A framework for soft-error-resilient sequential cell design by quantifying performance trade-offs in the *soft-error-resilience—power—delay—area* design space is presented, with a comprehensive silicon evaluation of representative circuit and layout techniques in 180 nm bulk CMOS.
2) A new soft-error-resilient sequential cell called LEAP-DICE is introduced. LEAP-DICE achieves the best soft error performance among selected sequential cell designs representative of existing soft-error-resilience circuit techniques. LEAP-DICE combines the SEU-immune **D**ual **I**nterlocked Storage **C**ell (DICE) circuit topology with a new SEMU-resilient layout principle called **L**ayout through **E**rror-**A**ware Transistor **P**ositioning (LEAP). It is the first example of soft-error-resilient circuit design, where circuit layout and transistor placement can improve the soft error performance of a circuit without significant area cost. As a result, LEAP-DICE offers 2,000X soft error resilience at moderate power and area costs compared to the reference D flip-flop.
3) Through the silicon validation of soft-error-resilience circuit techniques, new soft error effects related to circuit operating conditions such as voltage scaling, clock frequency setting and transistor aging (due to total dose effects) are discovered. These new effects should be considered in the design of soft-error-resilient sequential cells over the lifetime of their operation.

The rest of this paper is organized as follows. In Section II, circuit-level soft error resilience techniques that provide SEU immunity in flip-flops are investigated. In Section III, layout-level soft error resilience techniques aimed at reducing charge collection are illustrated. Section IV describes the test chip implementation used in this study. Section V presents the experimental setup and results, followed by conclusions in Section VI.

II. Circuit Techniques for Soft Error Resilience

Circuit techniques for soft-error-resilient sequential cells generally target soft errors due to upsets on a single circuit node. Circuit redundancy techniques provide an efficient way to reduce soft errors, by replicating identical circuit elements in the hope that a particle strike will only affect some but not all circuit elements, and the circuit can recover from partial failure by voting on the results of each replicated element [3]. *Dual Modular Redundancy* (DMR), a form of circuit redundancy, enables SEU immunity in the sequential cell design through the duplication of circuit elements [4]–[7]. Table I summarizes the various DMR circuit techniques to be discussed in the following subsections.

A. C-Element Based Soft-Error-Resilient Latches

The C-Element is a two-input comparator that passes the value of its inputs to its output when both inputs are equal, or maintains its previous output otherwise (Fig. 1). By using the

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TABLE I
CIRCUIT-LEVEL DUAL MODULAR REDUNDANCY (DMR) TECHNIQUES

Technique	Design	Redundancy Level
C-Element / Guard Gate	SCDMR [4]	Duplicated unprotected latches and additional C-Element voter with keeper.
	QCDMR [5]	Modified latch with guard gates (keeperless C-Elements) in duplicated feedback loop paths.
Differential Cascode Voltage Switch Logic	DIFF [6]	Differential (duplicated) circuit nodes for every logic gate.
Dual-Interlocked Storage Cell	DICE [7]	Modified latch with duplicated circuit nodes.

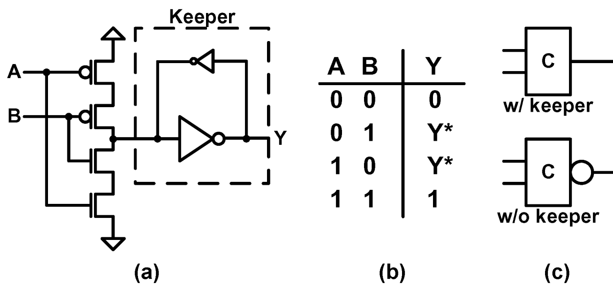

Fig. 1. C-Element. (a) Circuit implementation with optional keeper. (b) Truth table. (c) Symbolic representation [4].

C-Element to vote on the outputs of two identical latches, a soft-error-resilient latch called *Single C-Element DMR* Latch (SCDMR in Fig. 2(a)) can be constructed. This latch is similar to the BISER flip-flop [4] but without the scan structure, and is immune to single errors affecting any of its latches. However, it is susceptible to SEMUs involving either both latches, or one of the latches with the C-Element.

The SCDMR latch can also be modified by directly incorporating keeperless C-Element (also called *Guard Gates*) into the feedforward paths of the original latches to create a *Quadruple C-Element DMR Latch* (QCDMR in Fig. 2(b)), similar to the 4-TAG design from [5]. The QCDMR latch can only be upset when there are simultaneous errors involving both inputs of a C-Element.

B. Differential Cascode Voltage Switch Logic

The *Differential Cascode Voltage Switch Logic*, or DCVSL, provides a different DMR approach by replicating each signal with its complement (Fig. 3(a)) [6]. In DCVSL logic, all logic functions are implemented in its "NMOS-tree" structures, while PMOS devices simply serve as pull-up. As a result, the NMOS-tree structures are only sensitive to $0 \rightarrow 1$ transitions at their inputs. This special property prevents any SET on one circuit node from propagating beyond two logic stages (Fig. 3(b)). We implemented a DCVSL latch called "DIFF" (Fig. 3(c)) with an additional DCVSL 3-input C-Element at its output to prevent SETs in the internal circuit nodes from reaching the latch output. This circuit is vulnerable to SEMUs on any pair of differential signals (a signal and its complement) if the upset pulse width duration is larger than the loop delay of the circuit.

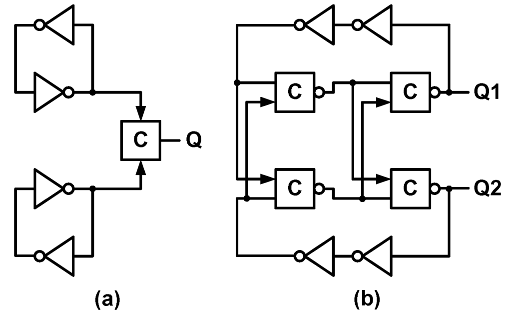

Fig. 2. C-Element based soft-error-resilient latches. (a) Single C-Element Dual Modular Redundancy (SCDMR) latch [4]. (b) Quadruple C-Element Dual Modular Redundancy (QCDMR) latch [5].

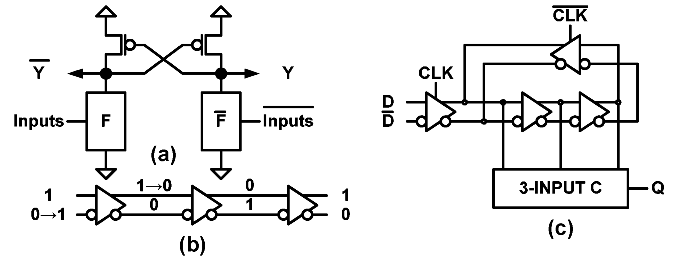

Fig. 3. Differential Cascode Voltage Switch (DCVSL) [6]. (a) Circuit implementation. (b) Single-event transient filter. (c) DCVSL latch "DIFF."

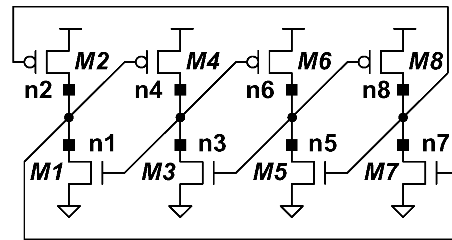

Fig. 4. Dual Interlocked Storage Cell (DICE) [7].

C. Dual Interlocked Storage Cell

The *Dual Interlocked Storage Cell*, or DICE, is a compact eight-transistor storage element relying on dual modular redundancy of its internal circuit nodes to achieve SEU immunity [7] (Fig. 4). When a particle strike temporarily upsets one circuit node resulting in an upsetting charge collection, only one additional circuit node in DICE is affected through circuit feedback. The two remaining circuit nodes can maintain their values, and with sufficient time can correct the values of the affected circuit nodes. However, the single node upset can lower the critical charge necessary to upset other unaffected circuit nodes, and the DICE circuit can become vulnerable to SEMUs through charge sharing.

III. Layout Techniques for Soft Error Resilience

A. Existing Layout Techniques

Past studies have shown that the placement of guard rings around active transistor area, especially around sensitive transistors, can lead to a reduction in single-event charge collection [8]. For circuits sensitive to SEMUs, doubling the distance between two sensitive circuit nodes can lead to a 10X reduction in the overall soft error rate [2]. In this study, all designs employ a standard cell layout design approach, with

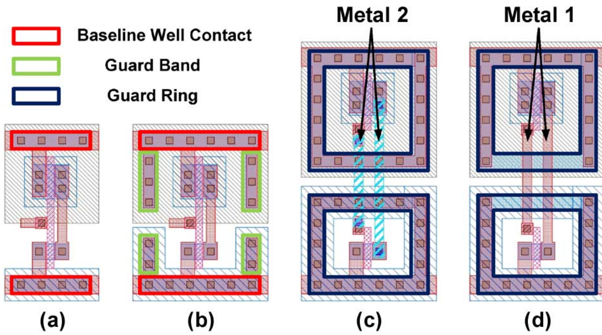

Fig. 5. Guard band and guard rings in CMOS inverter cell layout. (a) Common standard cell layout. (b) Common standard cell layout with vertical guard bands on the cell edges. (c) Fully contacted guard rings with metal 2 intra-cell wiring. (d) Partially contacted guard rings allowing the use of vertical metal 1 intra-cell wiring instead of metal 2 wiring. All designs in this work are implemented using the layout style in (d).

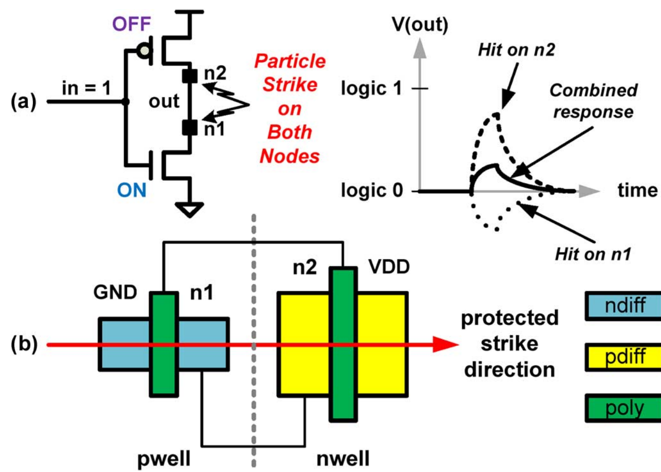

Fig. 6. LEAP principle for an inverter with transistor alignment. (a) Reduced charge collection when a particle hits both NMOS and PMOS drain nodes of an inverter simultaneously. (b) Transistor alignment to reduce charge collection in the horizontal direction [10].

guard rings surrounding each NMOS and PMOS active region. However, no explicit node separation is used to reduce the effect of SEMUs.

B. LEAP Principle for Soft Error Resilience

LEAP, or **L**ayout Design through **E**rror-**A**ware Transistor **P**ositioning, is a new layout principle for soft error resilience of digital circuits[1] [9], [10]. LEAP looks at the circuit response to SET charge collection at each individual diffusion contact node, then places the transistors in such a way that during a particle strike, multiple diffusion nodes can act together to fully or partially cancel the overall effect of the single event on the circuit.

For simplicity, let us consider the case where the drain contact nodes of the PMOS and NMOS transistors in an inverter are simultaneously hit by a particle strike. In the inverter example shown in Fig. 6, the positive charge collected by the PMOS transistor is offset by the negative charge collected by the NMOS transistor, resulting in lower total charge collection at the output node. Experimental results from [11] confirm this type of circuit interaction.

[1]LEAP was developed by Robust Chip Inc. with support from the Defence Threat Reduction Agency.

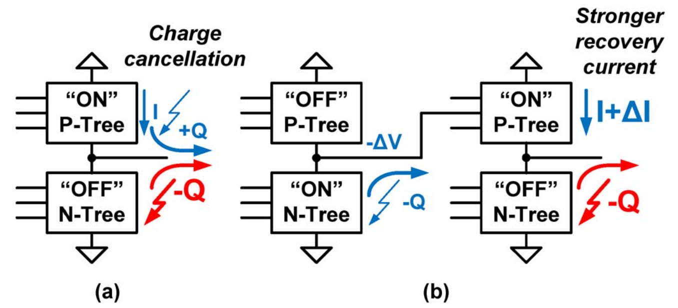

Fig. 7. Single-Event Transient (SET) suppression in a CMOS gate using the LEAP principle. (a) Direct LEAP SET Suppression. (b) Indirect LEAP SET Suppression. Charge collection that can result in a circuit offset is colored in red ("–Q" in this example). Charge collection that can enhance the circuit's soft error tolerance is colored in blue ("+Q" in this example).

In general, LEAP circuit interactions fall under two categories. In the first category, if a particle strike causes simultaneous charge collection in both "ON" and "OFF" trees ("+Q" and "$-$Q" in Fig. 7(a)) connected to the output of a CMOS logic gate, charge cancellation can occur at the output, reducing the probability of upset. Since the charge cancellation is a direct result of opposing charges being collected simultaneously, this effect is called *Direct LEAP SET Suppression*.

In a different setting involving two logic stages, a particle strike in the "ON" tree at the first stage can increase the drive strength of the "ON" tree at the subsequent stage due to larger input gate overdrive ("$-\Delta$V" in Fig. 7(b)), creating a stronger recovery current ("I $+$ ΔI") at the output of second stage and making that output more tolerant to possible upsetting charge collection ("$-$Q") in the "OFF" tree of the second stage. Since the two-stage circuit SET interaction does not involve direct charge cancellation, it is aptly named *Indirect LEAP SET Suppression*.

To apply the LEAP principle to enhance the soft error resilience of an already robust sequential circuit, the DICE design is chosen for its simple eight transistor configuration. Before deciding on how to place each transistor, circuit interactions inside DICE are studied. For example, given an initial DICE circuit state found in Fig. 8(a), if a particle strikes the diffusion nodes "n1" and "n8" of transistors M1 and M8, a single-event multiple upset can occur at all circuit nodes A through D (Fig. 8(b)). In contrast, if the particle strikes the diffusion nodes "n1" and "n2" instead, charge cancellation can happen through Direct LEAP interaction, preventing circuit node A from flipping its logic value. Here, node "n2" is denoted as a protective node for node "n1."

Since the DICE circuit is only sensitive to SEMU strikes involving at least two "sensitive" transistor drain nodes, for each possible SEMU path involving two sensitive transistor drain nodes (e.g. nodes "n1" and "n8" in Fig. 8), a "protective" transistor drain node (e.g. node "n2") is placed between the sensitive nodes to mitigate charge collection. In that way, every time both nodes in the sensitive node pair are struck simultaneously, the inserted protective node will also be struck, and the combined SET response (Fig. 8(b) & Fig. 8(c)) will reduce the effective SET response in the overall circuit.

Fig. 9(a) shows the standard DICE layout. Using LEAP, a new DICE flip-flop layout called LEAP-DICE is created (see

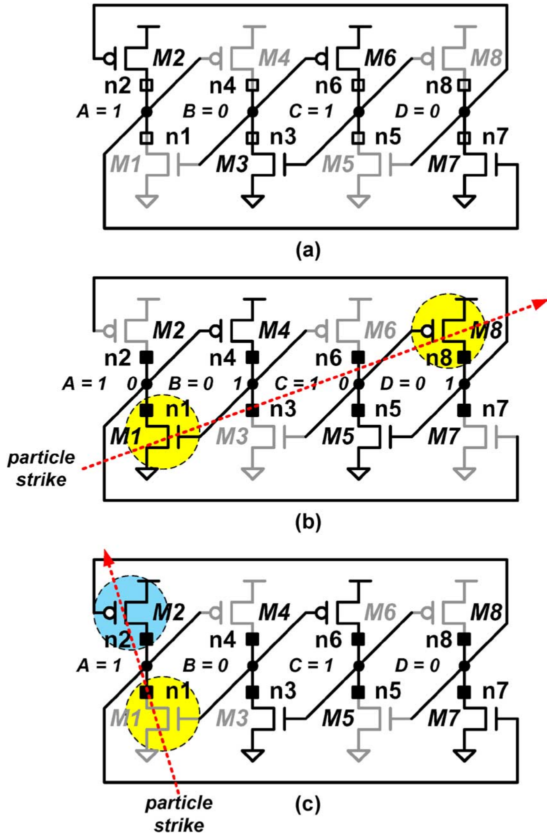

Fig. 8. Single-event charge collection in the Dual Interlocked Storage Cell (DICE). For simplicity, each "OFF" transistor is grayed off. (a) Initial state. (b) Simultaneous particle strike on transistors M1 and M8 results in an upset. (c) Simultaneous particle strike on both M1 and M2 results in charge cancellation (direct LEAP suppression) instead.

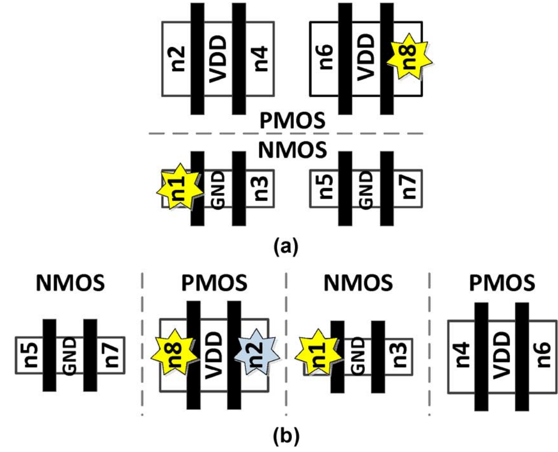

Fig. 9. Layout styles for the Dual Interlocked Storage Cell (DICE). (a) Conventional layout. (b) SEMU-resilient LEAP-DICE layout. The sensitive node-pair n1-n8 is highlighted in yellow. In LEAP-DICE, the protective node n2 (highlighted) in blue is positioned between the node pair [10].

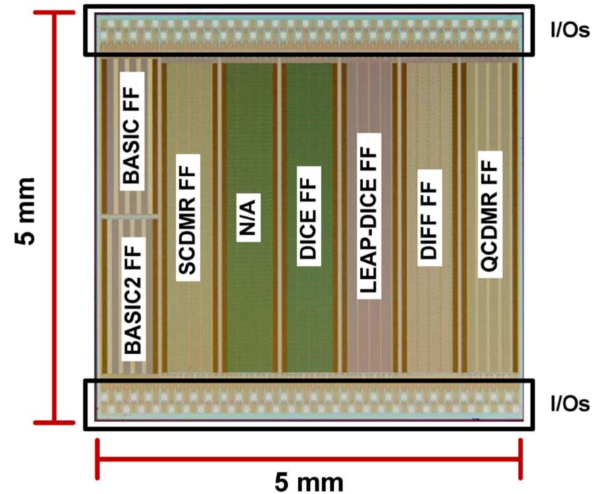

Fig. 10. Die photograph of the 180 nm bulk test chip.

Fig. 9(b)), by protecting SEMU strike directions involving any pair of two sensitive transistor drain nodes, through the positioning of another protective transistor drain node between them.

IV. Test Chip Implementation

To validate the soft error resilience of circuit and layout techniques discussed in Sections II and III, several flip-flop designs were implemented in a 5 mm × 5 mm 180 nm CMOS test chip (Fig. 10). Each design contains a minimum-size input inverter, a master latch, a slave latch and a minimum-size output inverter, with separate non-overlapping clocks for each master or slave stage. Scan chains of 2,304 to 4,608 flip-flops were implemented for each design. The test chip contains the following flip-flop designs:

1) BASIC: reference standard D flip-flop, with minimum-size transistors ($\mathrm{P/N} = 0.68\ \mu\mathrm{m}/0.28\ \mu\mathrm{m}$, $\mathrm{L} = 0.18\ \mu\mathrm{m}$).
2) BASIC2: same design as BASIC FF but with double transistor sizes for all transistors except in the input, output and clock inverters. It thus consumes 1.44X power (instead of 2X) and 1X area of BASIC as cell height remains unchanged.
3) SCDMR: flip-flop similar to SCDMR latch in Fig. 2(a), but replacing each latch with a BASIC flip-flop. The SCDMR flip-flop therefore comprises two BASIC flip-flops, with an output C-Element with keeper acting as SET filter.
4) QCDMR: master-slave flip-flop using the QCDMR latch design from Fig. 2(b).
5) DIFF: master-slave flip-flop using the DCVSL latch design from Fig. 3(c).
6) DICE: master-slave flip-flop using the DICE latch design from Fig. 4 with conventional layout from Fig. 5(a).
7) LEAP-DICE: master-slave flip-flop with circuit topology identical to the DICE flip-flop, but with the new LEAP-DICE layout from Fig. 5(b).

Table II lists the performance parameters for all designs from post-layout-extraction simulation, with the supply voltage set to 1 V and the non-overlapping clocks for the master-slave flip-flop designs set at 40 MHz. Each design drives a 4X minimum-size inverter load (included in power simulation), at about 0.4 in normalized power compared to BASIC.

V. Radiation Experiment Setup and Results

For this study, two sets of tests were performed following guidelines from the JEDEC89A Standard [12]:

TABLE II
NORMALIZED POST-LAYOUT SIMULATION PERFORMANCE FOR VARIOUS FLIP-FLOP DESIGNS AT 40 MHz and 1 V SUPPLY

Flip-Flop Design	Transistor Count	Layout Area	Power	Average Clock to Ouput Delay
BASIC	24	1.00	1.00	1.00
BASIC2	24	1.00	1.44	0.97
SCDMR	60	2.33	2.16	1.37
QCDMR	84	3.00	3.76	1.80
DIFF	56	2.42	3.37	2.48
DICE	52	1.67	1.50	1.06
LEAP-DICE	**52**	**2.33**	**1.54**	**1.07**

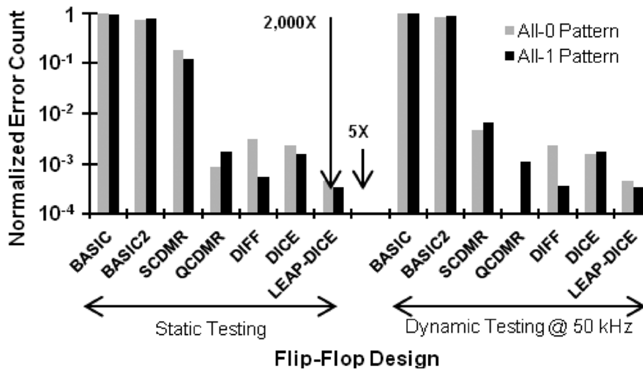

Fig. 11. Measured soft error performance of flip-flops at 1 V.

— *Static testing*: a test data pattern ("all 0 bits" or "all 1 bits") is first loaded into the flip-flops. Clocks are then disabled during irradiation while the test chip is still powered. After the irradiation reaches a certain *fluence* (number of particles passing through per unit area), the data pattern is read back by enabling the clocks again.

— *Dynamic testing*: the test data pattern is continuously loaded into flip-flops at a set frequency during irradiation while errors are counted. The "all 0 bits" and "all 1 bits" patterns are also used in this testing.

To evaluate the soft error performance of the different flip-flop designs, a neutron test was first conducted at Los Alamos National Laboratory (LANL). The LANL test beam has an energy profile similar to the neutron flux found at New York City Sea Level but with an acceleration factor of 3×10^8. The chips were irradiated at 0.8 V supply at normal incidence with a 3-inch beam diameter, and there was no observed latchup. Few errors were detected for the BASIC flip-flop (1 error per 2–3 hours of beam time), and none for the other designs.

To increase the number of observed errors, a second test was then performed at Indiana University Cyclotron Facility (IUCF) using a 3-inch diameter 200-MeV mono-energetic proton beam. The test chips were exposed at normal incidence up to 2 Mrad[Silicon] dose. Both static and dynamic testings were performed on the chips at 1 V, 1.4 V and 1.8 V. The observed number of errors remained fairly constant at 1 V, but increased during the course of the experiments at other voltages due to total dose effects similar to transistor aging. The observed soft error counts for all design with static and dynamic testing at 1 V are reported in Fig. 11.

The following notable observations were made from the radiation experiments:

1) LEAP-DICE has the best overall soft error performance among all designs, with on average 2,000X fewer errors compared to the reference BASIC design, and 5X fewer errors compared to the DICE design while sharing the same DICE circuit but with a different layout. LEAP-DICE requires 133% more area, 54% more power but negligible delay compared to BASIC.
2) It's interesting to compare the performance between DICE and LEAP-DICE in all dimensions of the *soft-error-resilience—power—delay—area* design space. Since both designs share the same circuit topology and transistor sizes, their power and delay numbers are literally identical, save for minor differences due to differences in parasitics caused by different internal wiring. LEAP-DICE requires roughly 40% more area than DICE, but improves the soft error resilience by 5X. Using the "$2\text{X node separation} = 10\text{X}$ fewer soft errors" rule of thumb from [2], a 40% area increase in the conventional DICE layout using proportional increase in node separation without any change in transistor placement will only result in 1.75X better soft error resilience. Therefore, node separation alone cannot fully explain the 5X soft error improvement in LEAP-DICE. This simple calculation shows that transistor placement can play an active role in making sequential circuits more robust without sacrificing too much layout area.
3) The doubling of internal transistor sizes in BASIC2 compared to BASIC barely improved the soft error rate, showing that making the transistors bigger alone is insufficient to make circuits robust.
4) The soft error resilience improvement using DMR circuit techniques falls within a range of values between 10X to 1000X, with the average hovering around 100X–200X. The SCDMR flip-flop was unexpectedly a lot softer compared to DICE, although both shared similar SEMU charge collection thresholds in simulation. The soft errors in SCDMR (Fig. 12(a)) were dominated by SEMU strikes involving the slave latch and the C-Element separated at 1 μm apart, while the DICE design is most sensitive to SEMUs involving circuit nodes with a 10 μm separation. To reduce the number of SEMUs, a new SCDMR layout arrangement (Fig. 12(b)) is proposed to physically separate the C-Element from the slave latch with negligible impact on area, power and delay. Other soft-error-resilient designs implemented in this study did not have node separation issues (most sensitive nodes were separated by at least 5 μm apart).
5) SCDMR encountered almost 100X more errors in static testing compared to dynamic testing. To investigate this difference, the SCDMR design was tested by varying the clock frequency in dynamic testing as well as changing the fluence steps in static testing by treating each fluence step in static testing as being equivalent to one single clock cycle in dynamic testing. Fig. 13 shows the combined result. At low fluence steps, the soft error count remains constant, as it is related to the cell SEMU probability where

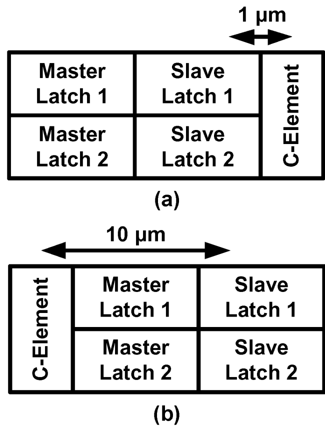

Fig. 12. SCDMR layout placement. (a) Original layout. (b) Proposed layout.

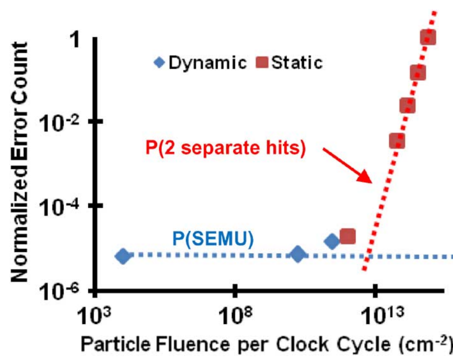

Fig. 13. SCDMR frequency response. The blue diamond points correspond to dynamic testing at 50 kHz, 0.5 Hz and 0.05 Hz, while the red square points correspond to static testing at 10, 25, 50, 100 and 200 krad[Si].

one particle hit simultaneously upsets two D flip-flops or one D flip-flop and the C-Element. At high fluence steps however, the soft error rate increases at a rate identical to the square of BASIC soft error rate, roughly equal to the probability that two independent BASIC flip-flops will get hit at the same time. Since the SCDMR flip-flop is made up of two (unprotected) BASIC flip-flops plus a C-Element acting as a SET filter at the output, it appears that the higher soft error rate in SCDMR at high fluence steps is dominated by two separate hits widely spaced in time on each of the two flip-flops (or one flip-flop and the C-Element). Although it is anticipated that the SCDMR flip-flop is vulnerable to SEMU hits as well as two independent single node hits resulting in an upset, this is the first ever demonstration that the soft error rate of the SCDMR flip-flop or similar designs can be highly influenced by the probability of two separate hits under high fluence steps. Since the higher soft error rate appeared in accelerated testing with extremely low equivalent clock frequency ($\ll$1 Hz), the results imply that designs similar to SCDMR should not be held in standby in a radiation environment, where the accumulated fluence during standby can approach the fluence steps used in static testing. The commonly used *Triple Modular Redundancy* (TMR) flip-flop, composed of three identical unprotected flip-flops voted by a three-input

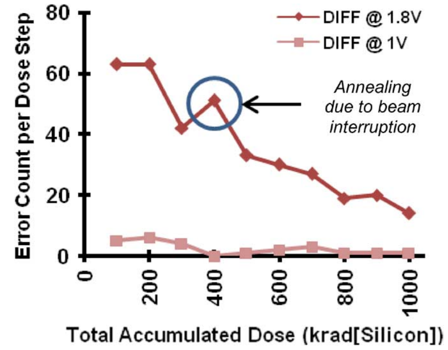

Fig. 14. Soft error reduction in the DIFF design with increasing accumulated radiation dose.

majority gate, also falls under the same category of sequential cells unsuitable for standby operation. Conversely, static testing is unsuitable to evaluate the soft error performance of aforementioned sequential cells during their normal (non-standby) operation.

6) The soft error count for most flip-flop designs increased around 20% by scaling down the supply voltages from 1.8 V to 1 V. The soft error count also increased slightly within 10% over large total dose exposure. In contrast, the DIFF design showed substantial soft error improvement in both cases (Fig. 14). The reason for this unexpected behavior can be traced to the combination of voltage scaling and total dose transistor aging exacerbating the already skewed rise/fall time ratio in DCVSL gates due to unbalanced P/N ratio (weak PMOS, strong NMOS). When the drive strength of NMOS devices become much stronger than that of the PMOS devices with total dose exposure, the gate delay slows down significantly due to slower PMOS feedback, making DCVSL gates substantially slower, but also preventing short-duration SET pulses from propagating and creating an upset.

To showcase the performance tradeoffs between the flip-flop designs, this work introduces a new metric called Soft Error Resilience, defined as follows:

$$\text{Soft Error Resilience} = \frac{1}{\text{Normalized Soft Error Rate}},$$

where the Normalized Soft Error Rate is defined as the soft error rate of a sequential cell in a study of various sequential cell designs under same operating conditions normalized by the maximum soft error rate found among all designs. By default, "Soft Error Resilience" is equal to 1 for the least soft-error-resilient design. Fig. 15 places each flip-flop design in the new "energy—area—soft-error-resilience" space, where the (switching) energy is defined as the power-delay product. LEAP-DICE is the most soft-error-resilient among all designs with moderate area and energy costs.

VI. Conclusion

Soft errors pose a major concern in circuit reliability with technology scaling. This study presents a design framework

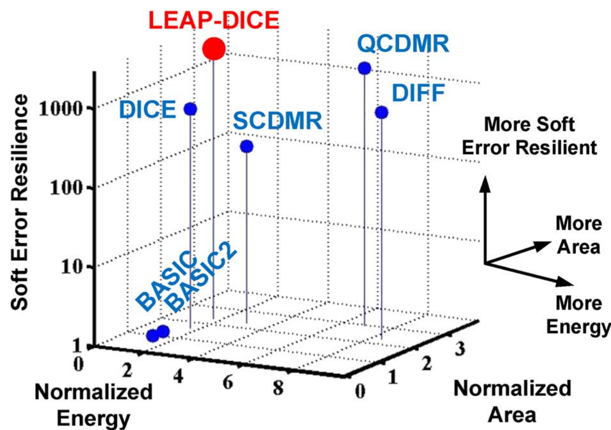

Fig. 15. Design framework putting LEAP-DICE and other soft-error resilient flip-flops in the energy—area—soft-error-resilience space. Energy (switching) refers to the power-delay product. All dimensions are normalized to BASIC.

for soft-error-resilient sequential cells in the soft-error-resilience—power—delay—space, with a silicon implementation of representative circuit and layout techniques. LEAP-DICE, which combines SEU-immune DICE circuit with SEMU-resilient LEAP layout principle, showcases how the best soft error performance can be achieved with 2,000X soft error resilience compared to the reference D flip-flop, at moderate area and power costs.

The LEAP-DICE example illustrates how a combination of circuit and layout techniques will be essential for the design of next generation sequential cells, as SEMU probability increases exponentially with device scaling. Newly discovered soft error effects from this study highlights the importance of including operating conditions as an essential factor in determining the robustness of a soft-error-resilient sequential cell during its lifetime of operation. As deep submicron device scaling makes transistors closer to each other than ever, future work in the area of soft-error-resilient sequential cell design can include a re-evaluation of the circuit and layout techniques surveyed in this work using the latest silicon process technology.

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