SINGLE-CHIP VLF MAGNETIC FIELD RECEIVER

A DISSERTATION
SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING
AND THE COMMITTEE ON GRADUATE STUDIES
OF STANFORD UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

Andrew Tronson
May 2014

© 2014 by Andrew Henning Tronson. All Rights Reserved.
Re-distributed by Stanford University under license with the author.

This work is licensed under a Creative Commons Attribution-Noncommercial 3.0 United States License.
http://creativecommons.org/licenses/by-nc/3.0/us/

This dissertation is online at: http://purl.stanford.edu/rt607vn7087

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Umran Inan, Primary Adviser

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Ivan Linscott

I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

Boris Murmann

Approved for the Stanford University Committee on Graduate Studies.

Patricia J. Gumport, Vice Provost for Graduate Education

This signature page was generated electronically upon submission of this dissertation in electronic format. An original signed hard copy of the signature page is on file in University Archives.

Abstract

Electromagnetic waves in the VLF frequency band from 300 Hz to 30 kHz are used to study the atmosphere, geolocate lightning, map subterranean features and provide navigation and timing signals. These waves can be generated by man-made sources, such as the VLF transmitters operated by the US Navy to communicate with submarines while they are submerged. They can also be generated by natural phenomena. For example, a lightning strike generates an impulsive signal known as a radio atmospheric. The interaction of these natural and man-made signals with the ionosphere, the magnetosphere, and the earth's electrical environment provides valuable data for scientific research.

To facilitate this research, the VLF signals must be received and stored for further analysis. Due to the unique nature of these signals, specialized receiver hardware is required to receive them. Currently the most widely deployed VLF receiver is the AWESOME receiver developed at Stanford University. This receiver offers excellent data quality, but it has a power dissipation of around 60 Watts. The high power dissipation can be a problem because some of the most desirable locations to deploy receivers are remote locations, which are far away from power-lines and other sources of electromagnetic interference. In these cases, the receiver must have a very low power dissipation as it must operate on battery power for long periods of time. Low-power VLF receivers for remote deployments have been developed, but their lower power dissipation comes at the expense of data quality. The goal and challenge of this research is to design a low-power receiver without sacrificing data quality.

To accomplish this goal, the first single-chip broadband VLF magnetic field receiver has been developed. The receiver consists of a low-noise amplifier (LNA) and

an analog-to-digital converter (ADC) integrated on a single-chip. The LNA is implemented using a low-impedance bipolar input stage followed by a variable gain differential instrumentation amplifier. The ADC is implemented with a third-order continuous-time delta-sigma modulator, which was selected for its implicit anti-alias filtering capability and its robustness to mismatch and other non-ideal effects. The receiver also includes an automatic biasing system that compensates for the large temperature variations that are often encountered at remote deployment sites. The receiver was fabricated in a 0.13 µm BiCMOS process and has a die area of 2.56 mm^2.

The LNA achieves a sensitivity of better than 1 $fT/Hz^{1/2}$ using a standard six-turn 4.9 meter square loop antenna. It also has a peak spurious-free dynamic range of up to 104.02 dB and a 3 dB bandwidth that extends from 170 Hz to over 100 kHz. The power dissipation of the LNA is approximately 908 µW. The on-chip delta-sigma ADC has an effective resolution of 12.40 bits and a spurious-free dynamic range of over 93 dB. The power dissipation of the ADC is roughly 640 µW. The full receiver consists of the combination of the LNA and the ADC and has a total power dissipation of approximately 1.55 mW.

A side-by-side comparison of field data from the single-chip receiver and the AWESOME receiver reveals that the data quality of the single-chip receiver is at least as good. Further, the single-chip receiver has a power dissipation that is over 30 times less than the current low-power receiver. The high data quality, low power dissipation and small size make the single-chip VLF magnetic field receiver especially well suited for remote VLF data collection.

Acknowledgements

Although there is only one person listed on the title page of this dissertation, there are many more who deserve recognition for helping to make this project a success. First and foremost, I would like to thank my research adviser Professor Umran Inan. Throughout my time at Stanford he has provided guidance, encouragement and unwavering support. I'd also like to thank Dr. Ivan Linscott who served as the co-adviser for this project. His technical contributions and feedback were invaluable. Additionally, I'd like to thank Professor Boris Murmann who reviewed this dissertation and provided many helpful suggestions. I would also like to thank Ahmad Bahai and Martin Lee at Texas Instruments. Not only did Texas Instruments generously provide funding to support this research, but they also invited us to use their well-equipped labs in Santa Clara to test the single-chip receiver described in this dissertation. Last but not least, I would like to thank my family and friends for their support and encouragement throughout my academic career.

Andrew Tronson
Stanford, California
May 30, 2014

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 VLF Research

Very low frequency (VLF) research covers a wide range of topics that includes the study of lightning, the atmosphere and other topics related to very low frequency electromagnetic waves [43, 53, 24, 35]. VLF refers to a band of frequencies that extends from 3 kHz to 30 kHz. Often in the course of these studies, signals that fall slightly above and below the VLF frequency band are also of interest. This extended frequency range includes the ELF (extremely low frequency) band that covers 300 Hz to 3 kHz and the LF (low frequency) band that covers 30 kHz to 300 kHz. For simplicity, in this dissertation the term VLF is used to refer to the frequency range from 300 Hz to 50 kHz, which includes the ELF frequency band, the VLF frequency band and the low end of the LF frequency band.

There are many sources of VLF radiation. These sources can be divided into two basic groups: man-made sources and naturally occurring sources. The man-made signals are generated by transmitters that broadcast in the VLF band. For example, VLF transmitters are used extensively by the US Navy to communicate with submarines while they are submerged. VLF signals are particularly well suited for this application because their low frequency allows them to penetrate into the water. The most common source of naturally occurring VLF radiation is lightning. In addition to thunder and a flash of light, a lightning strike also emits an impulsive

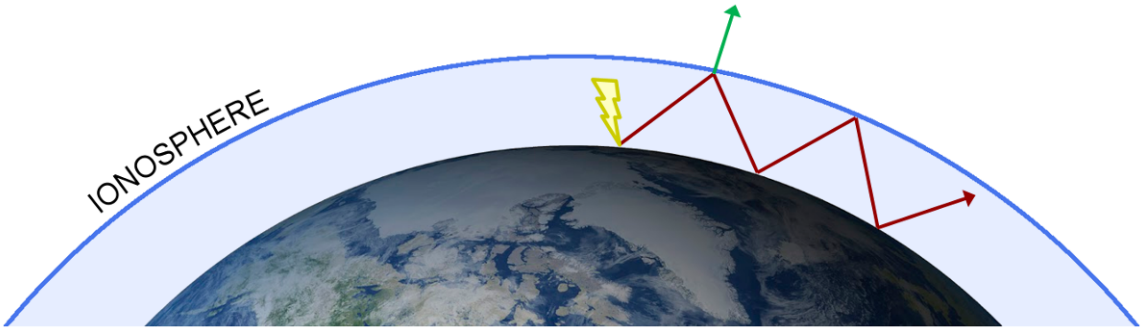


Figure 1.1: Lightning example showing VLF wave propagation in the Earth-ionosphere waveguide (red) and a wave escaping into the magnetosphere (green).

electromagnetic signal known as a radio atmospheric, or sferic for short [48]. A sferic has frequency components that reside primarily in the VLF frequency band.

An example of VLF wave propagation that results from a lightning strike is shown in Figure 1.1. In this example, a lightning strike occurs near the north pole and generates a sferic, the propagation direction of which is shown with the red line in the illustration. Due to the low frequency of the signal, it reflects off the earth and the ionosphere. As a result, the signal can travel extremely long distances in the so-called Earth-ionosphere waveguide. It is not uncommon to detect sferics from a lightning strike that occurred over 10,000 kilometers away [20]. In some cases the VLF radiation from a lightning strike can escape out of the ionosphere and into the magnetosphere, as shown with the green arrow in the figure. In this case, the wave travels along the magnetic field lines and can be detected at a geomagnetically conjugate point in the southern hemisphere.

Figure 1.2 shows an example spectrogram of VLF data collected by the Stanford VLF research group in Chistochina, Alaska [19]. A spectrogram is a plot which shows time on the horizontal axis and frequency on the vertical axis. The color represents the amplitude of the signal, where red corresponds to the largest signals and blue corresponds to the smallest signals. Essentially, a spectrogram shows the temporal variation of the dynamic spectrum of the signal.

The top plot in the figure shows 60 seconds of data over the frequency range of 0 Hz to 50 kHz, which is referred to as broadband VLF data because it covers the

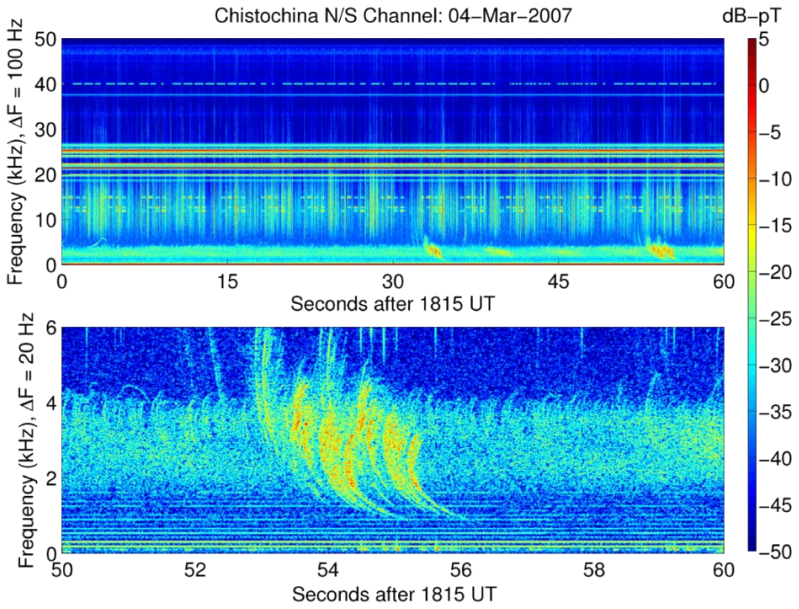


Figure 1.2: Example VLF data collected in Chistochina, Alaska in 2007. The top spectrogram shows broadband VLF data, which includes VLF transmitters and sferics. The bottom spectrogram zooms in on a whistler.

entire VLF frequency band. There are many different VLF signals visible in this spectrogram. Several strong VLF transmitters are visible between 20 kHz and 25 kHz. The transmitters broadcast in a small bandwidth around a constant frequency so they are easy to identify as horizontal lines in a spectrogram. The vertical lines that extend from roughly 5 kHz to 30 kHz are sferics, which are the impulsive signals generated by lightning strikes. Hundreds of sferics are visible in this data sample. This large number of sferics is not uncommon, as the average global lighting flash rate is approximately 50 flashes per second [16].

There is also an orange patch of signals in the lower right corner of the top spectrogram. The bottom plot zooms in on this area, showing only the data from 50 to 60 seconds over the frequency range of 0 Hz to 6 kHz. The curved signals in the middle of this zoomed spectrogram are called whistlers. These signals are detected when a VLF wave from a lightning strike escapes through the ionosphere into the magnetosphere, travels along the magnetic field lines and is received at a conjugate point in the opposite hemisphere. The signal has a curved shape due to the fact that

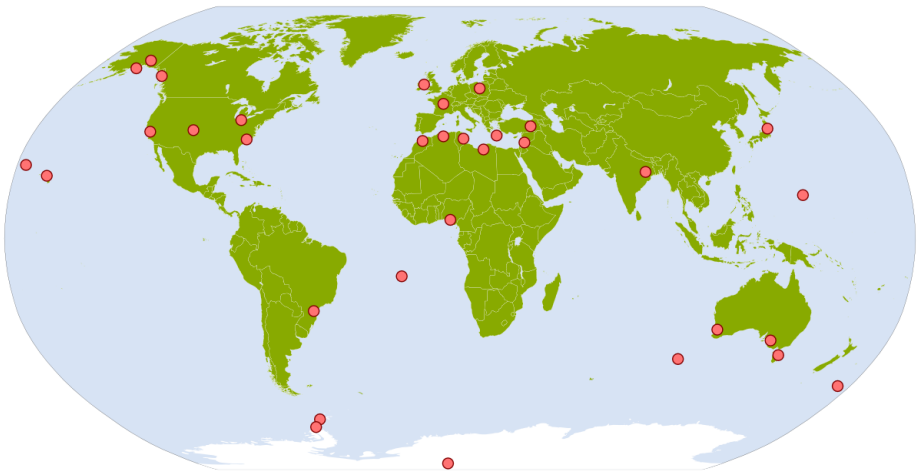


Figure 1.3: Map of VLF receivers deployed by the Stanford VLF research group.

the phase and group velocities in the ionized magnetospheric medium are functions of frequency. These signals are known as whistlers because they make a whistling sound when played on an audio speaker [30].

To facilitate the study of VLF phenomena, the Stanford VLF research group has developed several types of VLF receivers. These receivers are all custom designed for the unique requirements of receiving VLF waves. The two current models are the AWESOME receiver and the Penguin receiver. The AWESOME receiver is a high-performance VLF receiver, which receives signals with the highest data quality [19]. The Penguin receiver is a low-power VLF receiver designed for remote deployments at unmanned sites [32]. The Stanford VLF research group has deployed these receivers in dozens of locations around the world to collect data for scientific research. Figure 1.3 shows a map of the VLF receiver locations [36]. The receivers are deployed on all seven continents, including Antarctica. Many of the receivers are located in remote areas to minimize the amount of interference from power-lines and other sources of noise that are often found in urban environments.

The goal of this work is to develop the next-generation VLF receiver. This receiver should combine the high data quality of the AWESOME receiver with the minimal power dissipation of the Penguin receiver. At the same time, the next generation receiver is to be packaged in a single chip, to drastically reduce the size of the receiver

and open up new potential applications.

1.2 Contributions

The primary contributions of this work are:

1. Design, implementation and validation of the first single-chip broadband VLF magnetic field receiver.

2. Implementation of the first integrated VLF magnetic field low-noise amplifier that simultaneously achieves over 90 dB spurious-free dynamic range and under 1 $\mathrm{fT/Hz^{1/2}}$ sensitivity.

3. Demonstration of an automatic biasing system that increases the robustness of the low-noise amplifier to temperature variations.

4. Reduction of the signal path power consumption by over 30 times compared to the next-best low-power VLF receiver design.

1.3 Organization

This first chapter has provided a basic introduction to VLF science. It included an overview of the current network of VLF receivers deployed by the Stanford VLF research group and a description of some example VLF data that was collected with one of these receivers. It also included a summary of the primary contributions of this work. The remaining chapters are organized as follows.

Chapter 2 covers relevant background information and is divided into two parts. The first part gives a high-level overview of the various components of a VLF magnetic field receiver, which include the antenna, transformer and amplifier. This section also describes the methods used to test the receiver in a lab environment. The second part of this chapter reviews the basics of analog-to-digital conversion, with a focus on oversampling and delta-sigma modulation.

Chapter 3 gives a more detailed description of the VLF magnetic field receiver. It begins by discussing the key performance metrics, including the bandwidth, gain, sensitivity and spurious-free dynamic range. This is followed by a summary of the past VLF magnetic field receivers developed by the Stanford VLF research group. This chapter also includes a detailed discussion of the proposed single-chip receiver architecture and a comparison with the traditional receiver architecture. This chapter concludes by outlining the design specifications for the single-chip receiver.

Chapter 4 covers the circuit implementation of the single-chip receiver. This chapter describes the transistor-level design of all of the components of the receiver, including the low-noise amplifier and the analog-to-digital converter. It also provides a section dedicated to the design of the operational transconductance amplifier, which is a block that is used throughout the receiver. In addition, this chapter discusses several high-level receiver design issues, such as biasing and noise coupling.

Chapter 5 describes the measurement results of the single-chip receiver. It includes lab measurements of the performance of the low-noise amplifier and analog-to-digital converter, as well as measurements of the full receiver. Additionally, this chapter describes the field tests that were performed at Stanford University and at a quiet site in the Santa Cruz Mountains. This chapter concludes with a comparison of field test data between the single-chip receiver and the existing high-performance VLF receiver.

Chapter 6 summarizes the results of this work. This chapter provides a brief summary of the receiver design and the measurement results. It also includes a section that describes possible avenues for further research related to the single-chip receiver.

Chapter 2

Background

2.1 VLF Receiver Front-End

2.1.1 Antenna Design

A receiver can use one of two methods to detect an electromagnetic wave. It can use an electric field antenna, which is sensitive to the electric field of the received wave. Alternately, it can use a magnetic field antenna, which is sensitive to the magnetic field of the received wave. In the VLF frequency range the preferred method is to use an antenna that is sensitive to the magnetic field of the received signal [39]. The primary reason that a magnetic field receiver is used is because it has better noise performance at the low-end of the VLF frequency range when compared to a similarly designed electric field receiver. Additionally, a magnetic field receiver is simpler to calibrate as it is much less sensitive to nearby structures than its electric field counterpart.

The magnetic field antenna used in a standard VLF receiver is an air-core loop antenna. A model of the antenna is shown in Figure 2.1. It consists of a voltage source V_{a} that represents the antenna voltage induced by the incident wave, noise generator $\overline{v_{\mathrm{a}}^2}$ that represents the thermal noise of the antenna, resistor R_{a} that represents the resistance of the loop, inductor L_{a} that represents the inductance of the loop, capacitor C_{a} that represents the capacitance of the loop and resistor R_{r} that represents the

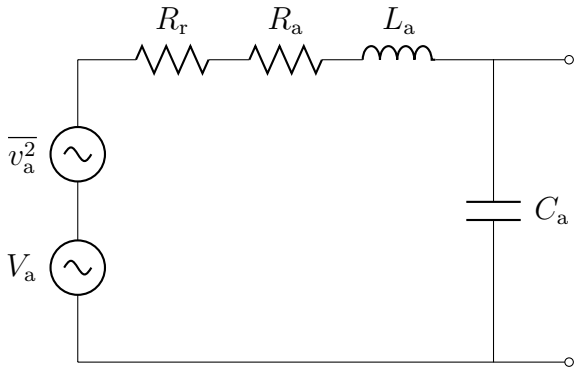


Figure 2.1: Model of the air-core loop antenna.

radiation resistance of the antenna.

In the VLF frequency band the radiation resistance is negligible because the loop is small compared to the wavelength of the received waves. The radiation resistance of the loop can be approximated by

$$R_r = 320\pi^4 \left(\frac{NA}{\lambda^2}\right)^2 \tag{2.1}$$

where N is the number of turns, A is the loop area and λ is the wavelength of the received wave [1]. With a frequency of 100 kHz and a standard six-turn 4.9 meter square antenna, the radiation resistance is approximately 8×10^{-6} Ω. This value is much smaller than the loop resistance of 1 Ω and can thus be safely ignored.

Similarly, the loop capacitance C_a is small and has a negligible effect on the antenna performance within the target bandwidth of the receiver. With the radiation resistance and the loop capacitance removed, the antenna impedance is given by

$$Z_a = R_a + j\omega L_a \tag{2.2}$$

which only depends on the loop resistance R_a and the loop inductance L_a.

A key metric of the loop antenna is the antenna turnover frequency, which is given by

$$f_a = \frac{R_a}{2\pi L_a} \tag{2.3}$$

At frequencies below f_a the antenna impedance is resistive. At frequencies above f_a the impedance is inductive. All of the loop antennas deployed by the Stanford VLF research group have a 1 Ω, 1 mH impedance, which results in a turnover frequency of approximately 159 Hz.

The voltage induced in the loop antenna by an incident electromagnetic wave can be calculated by using Faraday's law of induction, which states that the induced voltage is proportional to the rate of change of the magnetic field [11]. If a sinusoidal signal is assumed, then the induced voltage is

$$V_a = j\omega NAB_\omega \cos(\Theta) \tag{2.4}$$

where ω is the radian frequency of the wave, B_ω is the amplitude of the wave and Θ is the angle of incidence. Note that the induced voltage in the antenna is proportional to frequency. In all of the following analysis it is assumed that the incident wave is perpendicular to the antenna, so the cosine term is dropped. The magnetic field amplitude can be converted to an equivalent electric field amplitude using

$$E_\omega = cB_\omega \tag{2.5}$$

where c is the speed of light (3×10^8 m/s).

The antenna has two regions of operation. The first is the region below the antenna turnover frequency f_a, where the antenna impedance is resistive. In this region the output current from the antenna is proportional to frequency because the impedance is constant and the induced voltage is proportional to frequency. The second region of operation is above f_a, where the antenna is inductive. In this region the output current from the antenna is flat with frequency because the impedance is proportional to frequency and the induced voltage is proportional to frequency. The power of naturally occurring VLF signals is roughly constant over the entire VLF band, so it is desirable to operate the receiver in this flat region of the antenna above f_a. The 1 Ω, 1 mH loop antenna is used primarily because its turnover frequency falls below the start of the VLF band at 300 Hz.

Noise from the antenna originates from the thermal noise of the loop resistance

R_{a}. The noise power of the antenna can be expressed as

$$\overline{v_{\mathrm{a}}^2} = 4kTR_{\mathrm{a}}\Delta f \tag{2.6}$$

where k is the Boltzmann constant, T is the temperature and Δf is the bandwidth of the noise calculation [25]. This expression for the antenna noise can be used to calculate the sensitivity of the antenna when combined with Equation 2.4 for the induced voltage from an incident wave. Setting the noise voltage equal to the induced voltage and solving for the magnetic field amplitude B_ω results in an antenna sensitivity of

$$S_{\mathrm{a}} = \frac{\sqrt{4kTR_{\mathrm{a}}}}{\omega NA} \tag{2.7}$$

The antenna sensitivity is a measure of the minimum detectable signal and is defined as the magnetic field amplitude that results in a 0 dB signal-to-noise ratio at the output of the antenna when calculated in a 1 Hz bandwidth [39]. For a fixed antenna impedance, the antenna sensitivity can be improved by increasing the area of the loop. As a result, larger antennas generally have better sensitivities than smaller antennas. The sensitivity of the antenna decreases with increasing frequency. It is useful to remove this frequency dependence from the expression to aid in comparing the performance of different antennas. For this purpose, the normalized antenna sensitivity is defined as

$$S_0 = \frac{\sqrt{4kTR_{\mathrm{a}}}}{2\pi NA} \tag{2.8}$$

The actual sensitivity can be calculated from the normalized sensitivity by dividing by the desired frequency.

The loop antennas deployed by the Stanford VLF research group have a 1 Ω, 1 mH impedance. This impedance was chosen because the antenna turnover frequency falls well below the low-end of the VLF frequency band. An iterative approach can be used to generate antenna designs of various sizes and shapes that fit the 1 Ω, 1 mH impedance. Table 2.1 shows a selection of example designs and their normalized sensitivities [39]. The size of the square antennas refers to the length of each side of the square. The triangle antennas are right isosceles triangles where the size refers to

Table 2.1: VLF loop antenna designs with 1 Ω, 1 mH impedance.

Shape	Size m	Wire AWG	N	R_a Ω	L_a mH	f_a Hz	A m^2	S_0 V $Hz^{1/2}$ m^{-1}
Square	0.16	20	47	1.002	0.998	159.8	0.02563	5.03×10^{-3}
	0.567	18	21	1.006	0.994	160.9	0.3219	8.96×10^{-4}
	1.70	16	11	0.987	1.013	155.0	2.892	1.89×10^{-4}
	4.90	14	6	0.972	1.029	150.5	24.05	4.13×10^{-5}
Triangle	2.60	16	12	0.994	1.005	157.5	1.695	2.97×10^{-4}
	8.39	14	6	1.004	0.996	160.3	17.59	5.74×10^{-5}
	27.3	12	3	1.035	0.967	170.3	187.0	1.10×10^{-5}
	60.7	10	2	0.959	1.043	146.3	920.9	3.22×10^{-6}
	202	8	1	1.005	0.995	160.9	10164	5.97×10^{-7}

the size of the base (hypotenuse) of the triangle.

The antennas range from compact antennas that could be used with a hand-held receiver to large antennas that would be constructed to achieve the best sensitivity. Often the small antennas are used to survey an area for the optimal location to construct a large permanent antenna. The right isosceles triangle antennas are preferred for larger antenna deployments because they can be easily constructed with a single tower supporting the apex of the triangle. In this dissertation, for the purpose of calculating and comparing receiver performance, the 4.9 meter square antenna with six turns is used.

2.1.2 Receiver Design

The loop antenna is combined with a transformer and a low-noise amplifier to form the complete receiver front-end. Figure 2.2 shows the full model of the receiver front-end, including the loop antenna, which is modeled with a voltage source V_a that represents the induced voltage from an incident wave, a noise source $\overline{v_a^2}$, a loop resistance R_a and a loop inductance L_a. The antenna is followed by a 1:m transformer, which is assumed to be ideal in this analysis. The transformer is followed by a low-noise amplifier, which has a transimpedance gain of G and an input resistance of R_{in}. The receiver model also includes the input referred noise sources of the amplifier. The input referred

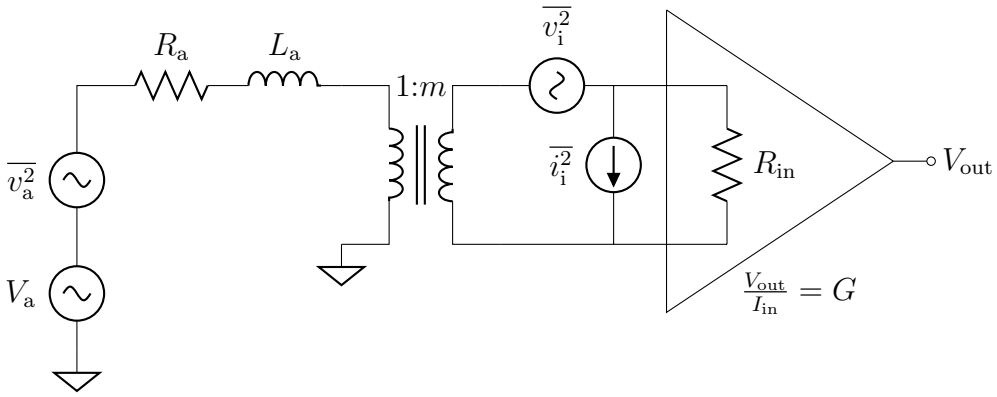


Figure 2.2: Model of the receiver front-end including the antenna, transformer, amplifier and noise sources.

voltage noise of the amplifier is represented by $\overline{v_i^2}$ and the input referred current noise of the amplifier is represented by $\overline{i_i^2}$.

The output voltage as a function of the antenna voltage can be calculated directly from the receiver model in Figure 2.2. The expression for the induced antenna voltage, given in Equation 2.4, can then be substituted to derive the output voltage as a function of the received magnetic field amplitude. The resulting relationship is

$$V_{out} = \frac{NAB_\omega G}{mL_a}\left(\frac{f}{f - jf_i}\right) \tag{2.9}$$

where f_i is the input turnover frequency and is given by

$$f_i = \frac{R_a + R_{in}/m^2}{2\pi L_a} \tag{2.10}$$

as shown in [39]. The input turnover frequency is the frequency at which the reactance of the loop is equal to the total resistance of the input circuit. Below f_i the output of the receiver is proportional to frequency. Above f_i the output of the receiver is flat with frequency. It is desirable to operate in the flat region, which is why a low input impedance amplifier is required. A typical design choice is to set $R_{in}/m^2 = R_a$, which results in $f_i = 2f_a$. In this case, the input turnover frequency is approximately 318 Hz with a 1 Ω, 1 mH antenna, which is right at the start of the VLF band.

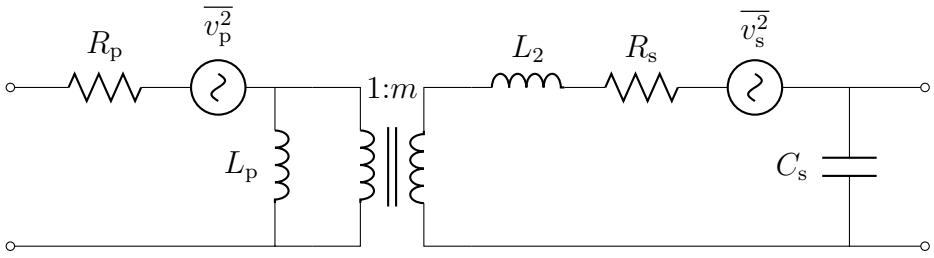


Figure 2.3: Model of the transformer including relevant parasitics.

The sensitivity of the receiver front-end can be calculated from the three noise sources included in the receiver model in Figure 2.2. The resulting sensitivity is

$$S_\mathrm{sys} = \frac{1}{\omega N A}\sqrt{\overline{v_\mathrm{a}^2} + \frac{\overline{v_\mathrm{i}^2}}{m^2} + \overline{i_\mathrm{i}^2} m^2 Z_\mathrm{a}^2} \tag{2.11}$$

At low frequencies the voltage noise sources dominate. However, over the majority of the VLF band the current noise is dominant because the antenna impedance $Z_\mathrm{a} \approx j\omega L_\mathrm{a}$. The current noise causes the sensitivity to flatten and reach a constant minimum value. As a result, the input referred current noise of the amplifier is critical to ensure good receiver sensitivity in the VLF band.

2.1.3 Transformer Design

The receiver front-end uses a hand-wound transformer to interface between the loop antenna and the input amplifier. A model of the transformer is shown in Figure 2.3. In addition to the ideal 1:m transformer, the model also includes the relevant parasitic elements. It includes the resistance of the primary winding R_p and the resistance of the secondary winding R_s, as well as their associated noise sources $\overline{v_\mathrm{p}^2}$ and $\overline{v_\mathrm{s}^2}$. The model also includes the inductance of the primary winding L_p and the leakage inductance referred to the secondary L_2. Finally, it includes the winding capacitance referred to the secondary C_s.

The transformer must be carefully designed to avoid degrading the performance of the receiver. The output voltage of the receiver as a function of the magnetic field

at the antenna with the full transformer model is given by

$$V_{\text{out}} = \frac{NAB_{\omega}G}{m\left(L_{\text{a}} + pL_2/m^2\right)} \left(\frac{f}{f - jf_{\text{t}}}\right) \left(\frac{f}{f - jf_{\text{i}}}\right) \left(\frac{-jf_{\text{c}}}{f - jf_{\text{c}}}\right) \tag{2.12}$$

where

$$f_{\text{t}} = \frac{\left(R_{\text{a}} + R_{\text{p}}\right) \parallel \left(R_{\text{s}} + R_{\text{in}}\right) p/m^2}{2\pi\left(L_{\text{a}} + L_{\text{p}}\right)} \tag{2.13}$$

$$f_{\text{i}} = \frac{R_{\text{a}} + R_{\text{p}} + \left(R_{\text{s}} + R_{\text{in}}\right) p/m^2}{2\pi\left(L_{\text{a}} + pL_2/m^2\right)} \tag{2.14}$$

$$f_{\text{c}} = \frac{1}{2\pi C_{\text{s}} R_{\text{in}}} \tag{2.15}$$

$$p = 1 + \frac{L_{\text{a}}}{L_{\text{p}}} \tag{2.16}$$

as shown in [39]. The transformer parasitics affect the frequency response of the receiver through the three corner frequencies shown above. The f_{t} corner was not present in the ideal transformer analysis and is the result of the effect of L_{p}, which reduces the gain of the receiver at low frequencies. The high frequency corner f_{c} is also new and is caused by the parasitic capacitance at the output of the transformer, which limits the bandwidth of the receiver. The input turnover frequency f_{i}, which was present before, is increased by the transformer parasitics.

All of the receivers deployed by the Stanford VLF research group use a hand-wound 24:548 turns ratio center-tapped transformer ($m = 22.83$). This turns ratio was selected because it provides a good balance between low frequency and high frequency noise performance [39]. For compatibility, this transformer is also used in the design of the single-chip receiver.

Figure 2.4 shows the frequency response of the receiver with the transformer parasitics included. A model of the 24:548 center-tapped transformer was used to generate

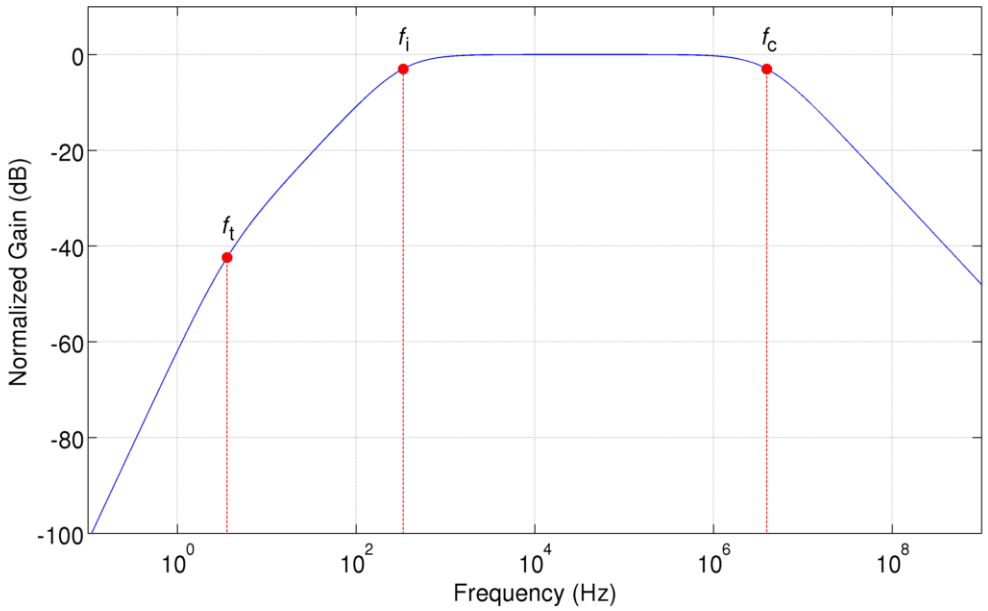


Figure 2.4: Receiver frequency response with the full transformer model.

this plot. The three corner frequencies are highlighted in the figure and occur at

$$f_t = 3.61 \text{ Hz}$$
$$f_i = 337 \text{ Hz}$$
$$f_c = 3.96 \text{ MHz}$$

The receiver is operated in the flat region of the response, which extends from roughly f_i to f_c or 337 Hz to 3.96 MHz. In a good design $f_t \ll f_i$ and f_c is larger than maximum frequency of interest. These goals are generally accomplished by designing the transformer to have a large L_p and a small C_s, as well as small parasitic resistances R_p and R_s. These conditions are satisfied by the 24:548 center-tapped transformer used by the single-chip receiver.

A center-tapped transformer offers two primary benefits. First, the center-tapped

transformer allows for the use of differential signaling throughout the receiver front-end, which rejects common-mode noise and interference, and reduces even-order harmonic distortion. Second, the center-tapped secondary winding allows for bias currents from the amplifier to pass through the transformer windings. Running bias currents in the windings is not a problem because the currents are balanced and create no net DC field in the transformer core. As a result, the receiver is much less sensitive to vibrations.

2.1.4 Amplifier Design

The frequency response and noise performance are the two primary design considerations for the front-end amplifier. The receiver frequency response is affected by the input resistance of the amplifier. Ideally, R_{in}/m^2 would be zero, which would result in the input turnover frequency being equal to the antenna turnover frequency. In this case, the receiver bandwidth would be maximized. However, this is not practical. A good compromise is to set $R_{\text{in}}/m^2 = R_{\text{a}}$. Given the predefined transformer turns ratio ($m = 22.83$), the necessary input impedance of the amplifier can be calculated. This calculation results in an input impedance of a few hundred ohms.

The noise performance of the amplifier is the second key design consideration. The amplifier noise can be characterized in terms of its input referred voltage noise and input referred current noise. Because of the inductive antenna impedance, the input referred current noise is dominant over most of the receiver bandwidth. As a result, minimizing the input referred current noise is critical to ensure good sensitivity of the overall receiver.

There are three basic types of amplifiers that can be used to achieve the impedance and noise goals. The first is a standard voltage amplifier with a physical resistor of value R_{in} terminating its input. While this meets the requirement for the input impedance, it has the worst noise performance of the three options. A well designed amplifier with an input impedance of R_{in} can have an input referred noise that is much lower than the noise of a physical resistor of value R_{in}.

The second amplifier option is a high impedance amplifier that uses current feedback to achieve a low input impedance. This architecture can achieve good noise performance if the feedback resistor and the forward gain are large enough. However, these requirements often lead to feedback stability issues that make this architecture not practical.

The third amplifier option is a low impedance amplifier, such as a BJT common-base amplifier or a CMOS common-gate amplifier. This is the preferred amplifier architecture because it has an inherently low input impedance and good noise performance. Generally the common-base amplifier is used due to its superior current efficiency and the lower $1/f$ noise of bipolar transistors [34]. One downside of using this amplifier architecture is that current noise at the output of the amplifier is referred directly to the input. This is because the common-base and common-gate amplifiers have a current gain of one. As a result, any circuits following the amplifier must be carefully designed to minimize their input referred current noise.

The front-end amplifier is implemented with a differential circuit architecture. As discussed in the previous section, this improves the common-mode rejection of the amplifier, balances the DC currents in the transformer windings and cancels even-order harmonic distortion [25].

2.1.5 Receiver Testing Methods

There are two methods of testing the receiver. The first is the induced signal method, where a second loop antenna is used to generate a known magnetic field that can then be received by the receiver's loop antenna. This method is problematic because it requires exact knowledge of the size, shape, position and orientation of the two loop antennas. The second method is the injected signal method, in which a known current is injected parallel to the antenna to simulate a received signal.

The injected signal method is preferred due to its accuracy and simplicity. Figure 2.5 shows the current injection circuit. It consists of a resistor R_{cal} and a capacitor C_{cal}. The figure also shows the antenna (R_{a}, L_{a}, V_{a}), the 1:m transformer, and the front-end amplifier. If R_{cal} is much larger than the impedance seen at the antenna

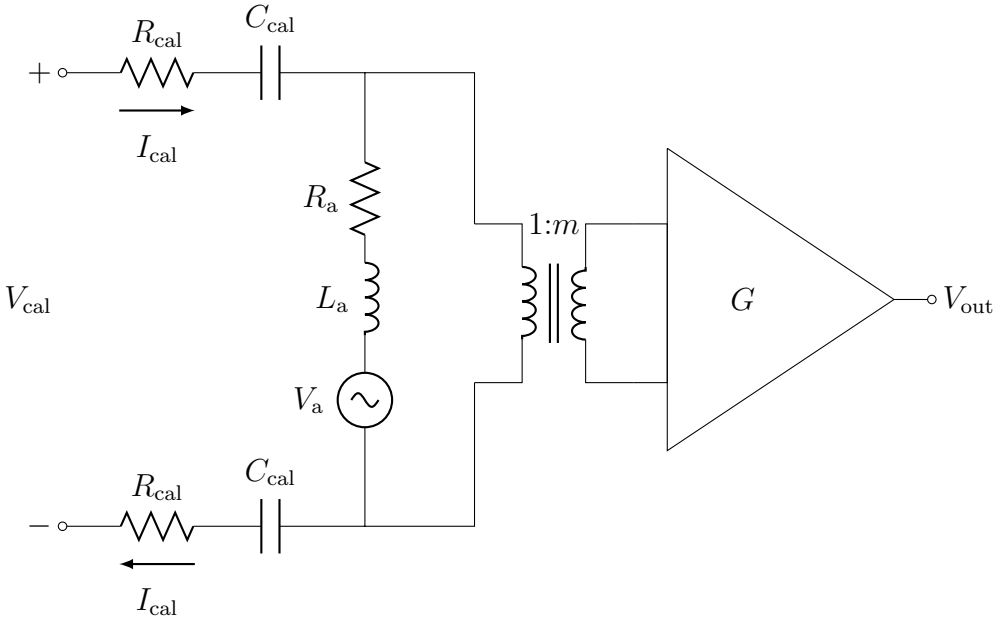


Figure 2.5: Receiver current injection circuit with the antenna, transformer and amplifier included for reference.

terminals, then the injected current I_{cal} only depends on the calibration resistor and capacitor

$$I_{\mathrm{cal}} = \frac{V_{\mathrm{cal}}}{R_{\mathrm{cal}}\left(1 + f_{\mathrm{cal}}/jf\right)} \tag{2.17}$$

where

$$f_{\mathrm{cal}} = \frac{1}{2\pi R_{\mathrm{cal}} C_{\mathrm{cal}}} \tag{2.18}$$

Essentially, the calibration resistor and capacitor convert the differential input voltage into a differential current that is injected in parallel with the loop antenna.

The calibration voltage that is equivalent to a magnetic field amplitude of B_ω at the antenna can be calculated with

$$V_{\mathrm{cal}} = \frac{NAR_{\mathrm{cal}}B_\omega}{L_{\mathrm{a}}} \frac{1 + f_{\mathrm{cal}}/jf}{1 + f_{\mathrm{a}}/jf} \tag{2.19}$$

If $f_{\mathrm{cal}} = f_{\mathrm{a}}$ then the frequency dependence of this relationship cancels. This is

accomplished by setting the calibration capacitor to

$$C_{\text{cal}} = \frac{L_{\text{a}}}{R_{\text{a}} R_{\text{cal}}} \tag{2.20}$$

With a properly selected calibration capacitor, the relationship between the calibration voltage and the magnetic field amplitude simplifies to

$$V_{\text{cal}} = \frac{NAR_{\text{cal}} B_{\omega}}{L_{\text{a}}} \tag{2.21}$$

Notice that the relationship is independent of frequency. It also does not depend on circuit parameters, such as the input impedance of the amplifier. This relationship can be used to convert a given calibration voltage into an equivalent magnetic field amplitude, assuming a particular antenna size and number of turns.

For testing purposes the loop antenna in Figure 2.5 can be replaced with equivalent passive components. This so-called dummy loop consists of a 1 Ω resistor and a 1 mH inductor. The dummy loop provides the same impedance as an actual antenna, but greatly reduces the amount of noise and interference that couples into the receiver. This is particularly important in a lab setting where an actual loop antenna would pick up a large amount of interference from nearby measurement equipment.

2.2 Delta-Sigma Analog-to-Digital Conversion

2.2.1 Analog-to-Digital Conversion

An analog-to-digital converter (ADC) is a device that converts a continuous signal, such as a voltage or current, into a digital value that represents the amplitude of the signal. Real world signals are analog, which means that they are continuous in time and amplitude. Analog-to-digital conversion is often used to take advantage of the benefits of digital signal processing (DSP). DSP provides immunity to noise and interference, enables error detection and data compression and allows for reconfigurability. Further, digital circuits can typically be designed and manufactured at a much lower cost than equivalent analog circuits.

An ADC performs two operations: sampling and quantization. The majority of ADCs use uniform sampling where the analog signal is sampled at a constant interval in time. For example, an ADC with a 1 MHz clock rate will sample the input every 1 µs. There has been research into non-uniform sampling, but it will not be considered here [6]. Assuming uniform sampling, the required sampling rate can be related to the bandwidth of the input signal through the Nyquist sampling theorem, which states that the original analog signal can be reconstructed from the digital values if

$$f_s \geq 2f_B \tag{2.22}$$

where f_B is the bandwidth of the input signal and f_s is the sampling frequency [38]. The Nyquist theorem states that the sampling frequency must be at least twice the bandwidth of the input signal. Often the sampling rate is set higher than the minimum value to allow room for the anti-alias filter to roll-off.

Quantization is the process of converting the amplitude of the input signal into discrete digital values. Because there are a finite number of quantization levels and the input signal is continuous, there will always be some error introduced in the quantization process. Figure 2.6 shows the quantizer transfer curve for a 3-bit ADC. The horizontal axis represents the input signal from -1 to $+1$ and the vertical axis represents the 8 digital values. The blue curve shows the transfer characteristic of the 3-bit ADC and the red curve shows the characteristic of an ideal infinite resolution ADC. Notice that error is introduced by the 3-bit ADC because there are only 8 digital output values but an infinite number of possible input values.

The full scale range of the ADC is defined as the range of the input signal that doesn't cause saturation. In this example the full scale range extends from -1 to $+1$. The step size Δ of the ADC is the width of the steps in the transfer curve. The step size can be calculated with

$$\Delta = \frac{FS}{2^B} \tag{2.23}$$

where FS is the full scale range and B is the resolution of the ADC. Therefore, higher resolution ADCs will have smaller step sizes.

Figure 2.7 shows the error of the quantizer, which is related to the difference

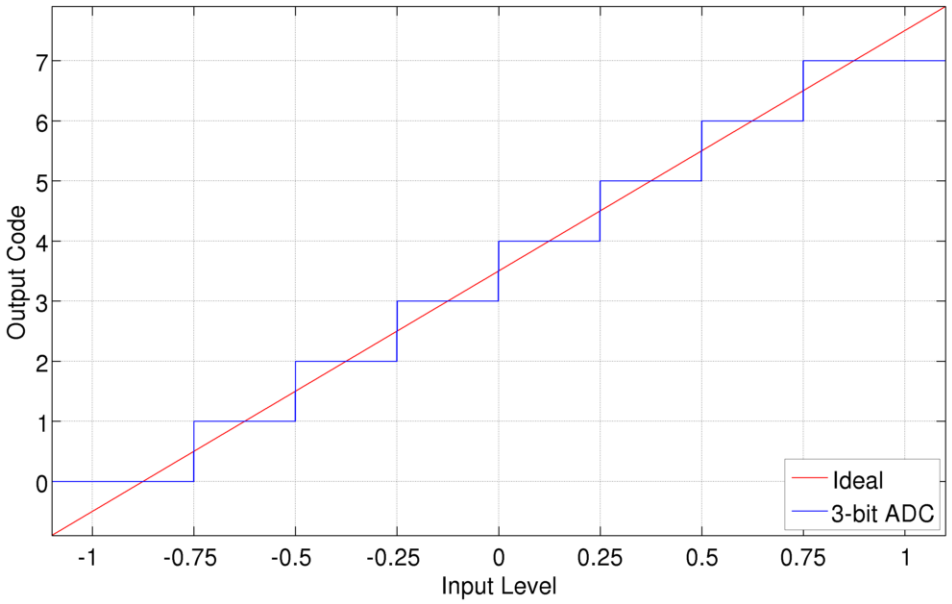


Figure 2.6: Quantizer transfer curve for a 3-bit ADC.

between the ideal infinite resolution ADC transfer curve and the 3-bit ADC transfer curve. Notice that the error is bounded between $-\frac{\Delta}{2}$ and $+\frac{\Delta}{2}$ for input signals from -1 to $+1$. Outside of this range the error increases without bound. This is caused by the input signal saturating the ADC.

If the input signal is sufficiently active and exercises a large range of digital codes then the quantization error can be assumed to be statistically random, which produces a white noise spectrum. The total quantization noise power is

$$\overline{e_{\mathrm{q}}^2} = \frac{\Delta^2}{12} \tag{2.24}$$

which is calculated by summing the noise components over the entire ADC bandwidth [38]. The total quantization noise power depends only on the step size of the ADC, which is related to its resolution, and not on the sampling rate of the ADC.

Figure 2.8 shows an example of the output spectrum of an 8-bit ADC with a sinusoidal input signal. The horizontal axis corresponds to frequency from 0 to $f_{\mathrm{s}}/2$ and the vertical axis is the amplitude of the signal. The large tone in the spectrum is

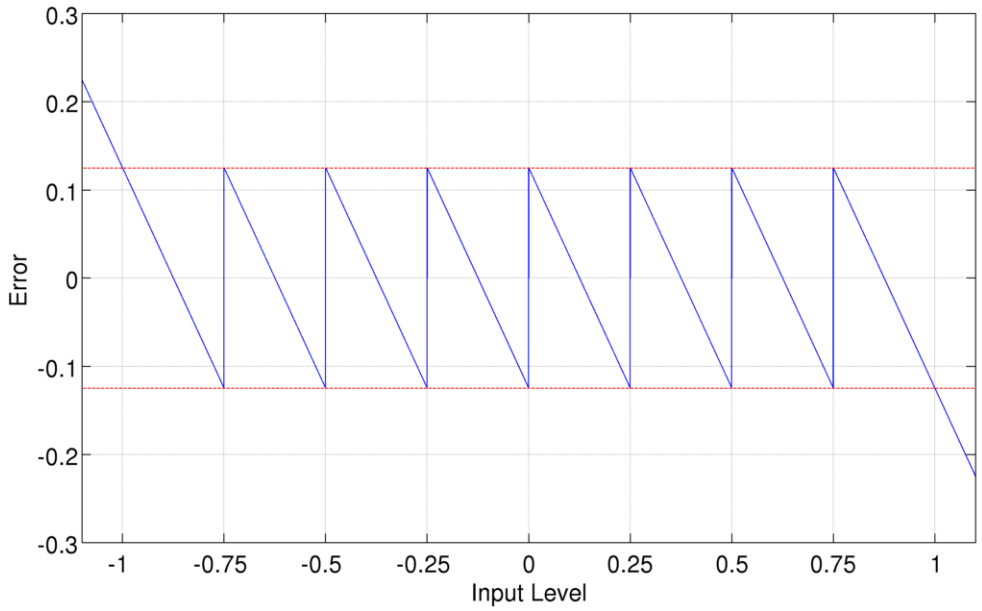


Figure 2.7: Quantization error for a 3-bit ADC.

the input sinusoid and the other small tones are the quantization noise components. Notice that the quantization noise spectrum is roughly flat over the ADC bandwidth, which agrees with the white noise approximation.

The performance of an ADC can be characterized in terms of its signal to quantization noise ratio (SQNR). The SQNR is calculated by taking the ratio of the signal to the sum of the quantization noise components, which can be related to the resolution of the ADC with

$$SQNR = 10 \log \left(\frac{P_{\mathrm{s}}}{P_{\mathrm{n}}} \right) = 6.02B + 1.76 \tag{2.25}$$

Therefore, the SQNR is directly related to the resolution, B, of the ADC. Higher resolution gives a larger SQNR and lower resolution gives a smaller SQNR. In the example spectrum in Figure 2.8 the SQNR is equal to 50.07 dB, which is very close to the 49.92 dB value predicted by Equation 2.25 for an 8-bit ADC. This equation can be inverted to calculate the resolution of the ADC from a given SQNR value. The

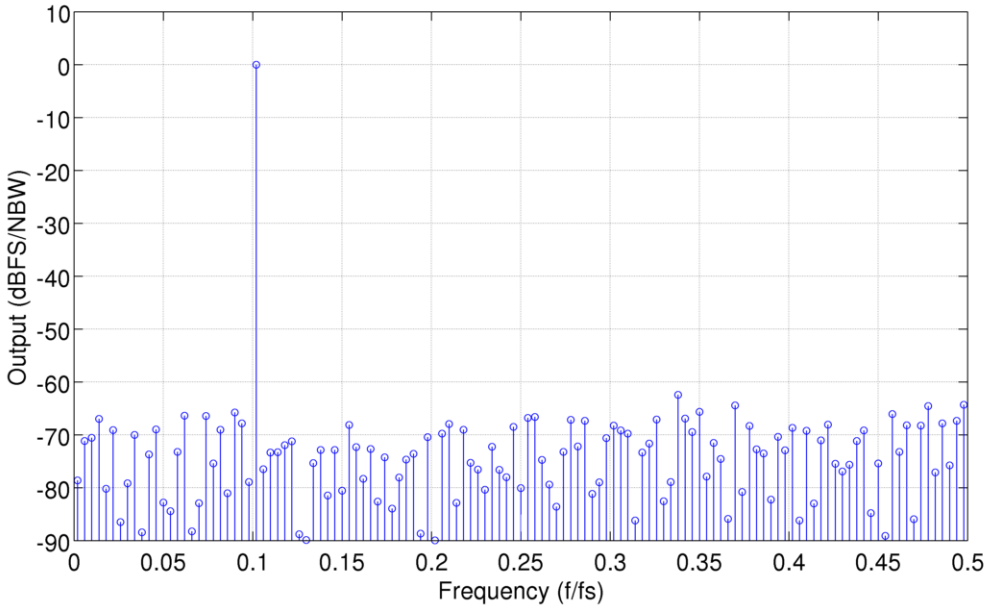


Figure 2.8: ADC output spectrum illustrating the distribution of quantization noise.

effective number of bits is

$$ENOB = \frac{SQNR - 1.76}{6.02} \tag{2.26}$$

where the SQNR is given in dB. This relationship is particularly useful for oversampled ADCs where the effective number of bits is not necessarily equal to the number of bits that the ADC outputs.

2.2.2 Oversampling

Oversampling refers to using a sampling frequency that is higher than the Nyquist rate. The oversampling ratio (OSR) is defined as

$$OSR = \frac{f_s}{2f_B} \tag{2.27}$$

where f_s is the sampling frequency and f_B is the bandwidth of the input signal. Oversampling has two primary benefits. First, an oversampled ADC has relaxed

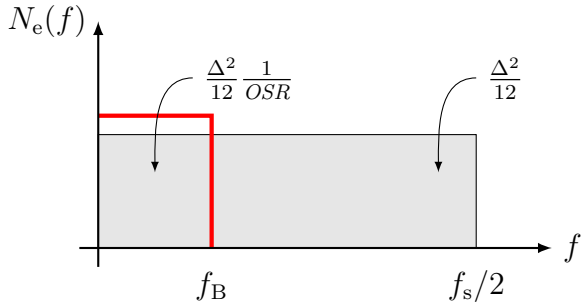


Figure 2.9: Example of oversampling. The red box is the desired ADC bandwidth.

requirements on the anti-alias filter because immediate roll-off is not needed. Second, the effective number of bits of the ADC is increased by oversampling because the total quantization noise is not dependent on the sampling rate. To illustrate this point, Figure 2.9 shows the quantization noise spectrum of an ADC. The noise is spread uniformly over the ADC bandwidth from 0 to $f_s/2$, but only the spectrum up to f_B is of interest if oversampling is used. The total quantization noise of the ADC is $\Delta^2/12$ and since it is spread over a larger bandwidth the quantization noise that falls below f_B is reduced. The in-band quantization noise is

$$\overline{e_q^2} = \frac{\Delta^2}{12}\frac{1}{OSR} \tag{2.28}$$

The quantization noise that falls outside the signal bandwidth can be filtered using a digital filter.

Oversampling improves the SQNR of the ADC, which results in a higher effective number of bits. In fact, each doubling of the sampling frequency results in an increased resolution of approximately 0.5 bits [45]. For example, consider an 8-bit ADC that is oversampled to produce a 12-bit effective resolution. To increase the resolution by 4 bits the sampling rate would have to be increased by a factor of 256. While this is possible, it may not be practical. As a result, oversampling to increase the effective resolution of an ADC is usually not done. However, oversampling to relax the requirements on the anti-alias filter is common.

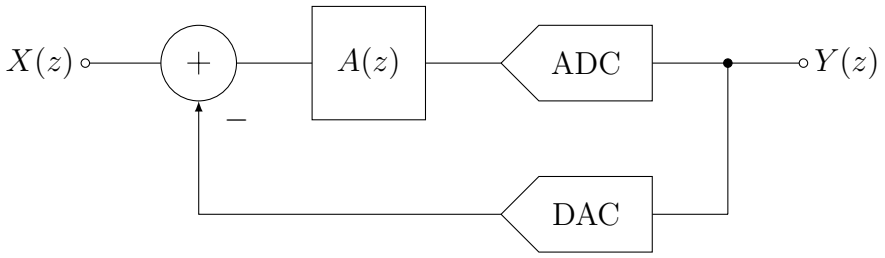


Figure 2.10: Block diagram of a discrete-time delta-sigma modulator.

2.2.3 Delta-Sigma Modulators

A delta-sigma modulator is an oversampling ADC architecture that operates on the principle of shaping the quantization noise spectrum away from the signal band so that it can later be removed by a digital filter [27]. This enables higher resolutions to be achieved while simultaneously relaxing the requirements on the analog components. In the previous section it was shown that basic oversampling can increase the resolution of an ADC, but significant increases in resolution require impractical sampling rates. The delta-sigma modulator overcomes this limitation by shaping the noise spectrum.

A block diagram of a delta-sigma modulator is shown in Figure 2.10. The modulator includes a discrete-time loop filter $A(z)$, a low resolution ADC that quantizes the signal and produces the digital output value, and a DAC that converts the digital output value to an analog value and feeds it back to the input of the modulator. The input to the modulator is a discrete-time analog signal, which means that $X(z)$ is a sampled version of the original input signal. The output signal $Y(z)$ is a discrete-time digital signal.

To understand the operation of the delta-sigma modulator it can be converted to a linear model, which is shown in Figure 2.11. The ADC is replaced by a summation node that adds noise from a noise source $E(z)$. This noise source corresponds to the quantization noise generated by the ADC at this point in the modulator. The DAC is assumed to be ideal in this analysis and is replaced by a direct connection from the output to the input summation node. Calculating the output as a function of the

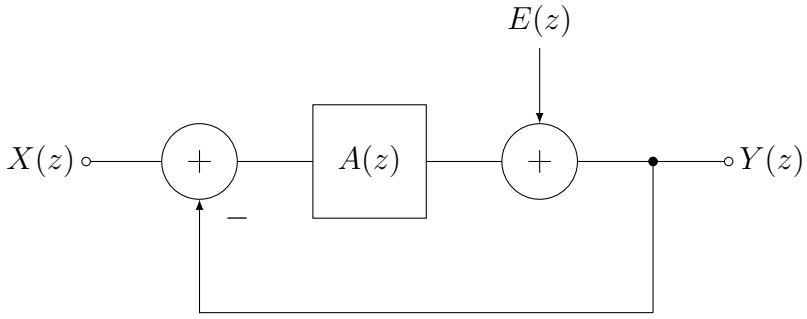


Figure 2.11: Linear model of a delta-sigma modulator.

input signal $X(s)$ and the quantization noise $E(z)$ yields

$$Y(z) = \frac{A(z)}{1 + A(z)} X(z) + \frac{1}{1 + A(z)} E(z) \tag{2.29}$$

The term preceding the input signal is referred to as the signal transfer function (STF) and the term preceding the quantization noise is called the noise transfer function (NTF).

The fact that the STF and the NTF are different can be exploited to shape the quantization noise spectrum. For example, consider the case in which the loop filter, $A(z)$, has a large gain at low frequencies. In this case, at low frequencies the STF would approach one while the NTF would approach zero. This means that a low frequency signal would pass through the modulator unchanged while the quantization noise at low frequencies would be significantly attenuated.

A common loop filter implementation is a discrete-time integrator. An integrator produces the desired transfer function, with a very high gain at low frequencies. The transfer function of a discrete-time integrator is

$$A(z) = \frac{z^{-1}}{1 - z^{-1}} \tag{2.30}$$

with this loop filter transfer function the output of the delta-sigma modulator becomes

$$Y(z) = z^{-1} X(z) + \left(1 - z^{-1}\right) E(z) \tag{2.31}$$

In this case, the STF is simply a one sample delay and the NTF is a high-pass filter. Assuming that the delta-sigma modulator is oversampling the input signal, then signals within the signal band (0 to f_{B}) are passed unchanged while the noise in the signal band is filtered and pushed to higher frequencies. The configuration with a single integrator as the loop filter is called a first-order modulator and results in first-order noise shaping. It can be shown that first-order noise shaping results in an increase in the effective resolution of the ADC of 1.5 bits for each doubling of the sampling rate. For example, if the internal ADC has a resolution of 4 bits and an oversampling ratio of 16 is used, then the effective resolution of the first-order modulator is increased by 6 bits for a total resolution of 10 bits.

In addition to using a higher oversampling ratio to increase the effective resolution, there are several other design strategies that can be used to increase the resolution of the delta-sigma modulator [45]. One common modification is to use a higher order loop filter. The previous example used a first-order loop filter, but higher order loop filters are possible. If a second-order loop filter is used then the transfer function of the modulator becomes

$$Y(z) = z^{-2}X(z) + \left(1 - z^{-1}\right)^2 E(z) \tag{2.32}$$

The input signal is still transfered to the output with only a delay, but now the quantization noise is filtered with a second-order high-pass filter. The higher order filter provides more quantization noise attenuation in the signal band and results in a higher SQNR. In fact, with a second-order loop filter the effective resolution of the ADC is increased by 2.5 bits for each doubling of the oversampling ratio.

This concept can be extended to an Nth-order loop filter, which result in an increased resolution of $N + 0.5$ bits for each doubling of the oversampling ratio [45]. However, there is a trade-off with increasing the filter order. Higher order modulators are more prone to instability, so precautions must be taken in their design. As a result, there are diminishing returns to increasing the modulator order above a certain point, which typically occurs around 5th or 6th order loop filters.

Another parameter of the delta-sigma modulator is the resolution of the internal

ADC. Typically only low resolution quantizers are used for the internal ADC, which have resolutions in the range of 1 to 4 bits. Using a resolution larger than 1 bit for the internal quantizer has two benefits. First, it provides a higher starting point for the resolution of the modulator. As a result, a lower oversampling ratio can be used to achieve the same resolution. Second, a higher resolution internal ADC improves the stability of higher order modulators.

However, there is one major drawback to using an internal ADC with a resolution greater than 1 bit. The problem arises because the feedback DAC, which uses the same resolution as the internal ADC, has to have the same accuracy as the overall modulator [38]. This is because the signal from the DAC is added directly to the input signal. For example, if a 4-bit internal ADC is used to build a 16-bit modulator, then the 4-bit DAC needs to have 16-bit accuracy. This requirement severely limits the performance of the modulator because it is difficult to build a DAC with linearity that matches the high resolution of the modulator. There are techniques to overcome this problem, such as dynamic element randomization and mismatch error shaping, but these methods add complexity to the design and consume additional power [8, 2]. As a result, single-bit internal ADCs are often used. This is because a 1-bit DAC is perfectly linear as it has only two levels.

To illustrate the operation of a delta-sigma modulator, a time-domain simulation of a single-bit third-order modulator is shown in Figure 2.12. The red curve is a sinusoidal input signal with an amplitude of -6 dB relative to full-scale (dBFS). The blue curve is the 1-bit digital output signal from the modulator. Notice that the output signal has a pulse-width modulation characteristic, in which the output signal has more $+1$ values when the input signal is high and more -1 values when the input signal is low.

The output spectrum can be calculated using the fast Fourier transformer (FFT) to visualize the effect of the quantization noise shaping. Figure 2.13 shows the output spectrum of the single-bit third-order delta-sigma modulator. An 8192 point FFT was computed with a Hann window to prevent spectral smearing. The tone from the sinusoidal input signal is clearly visible near the middle of the plot with an amplitude of -6 dBFS. The remainder of the spectrum is the quantization noise. Notice that

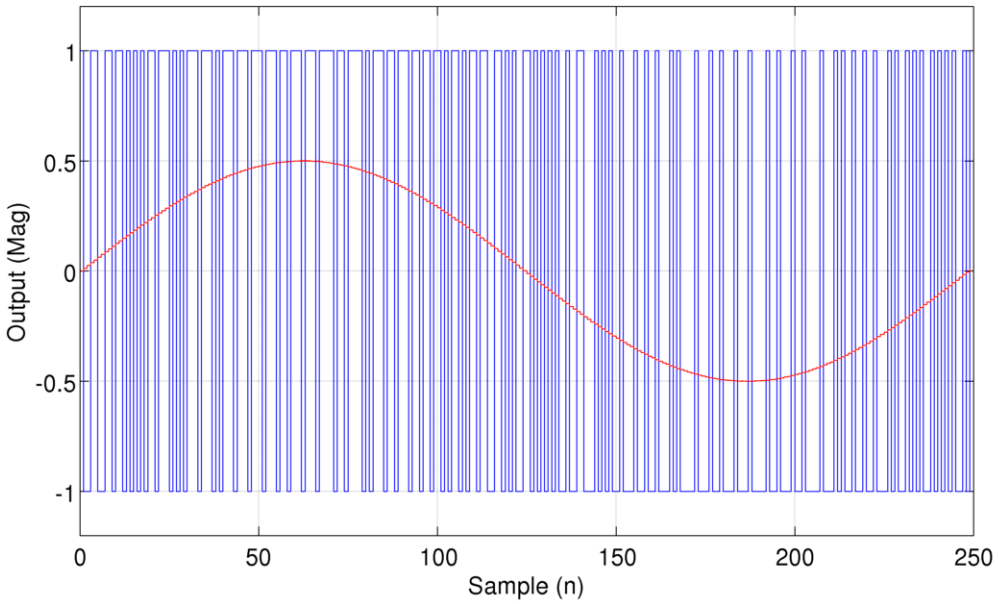


Figure 2.12: Time-domain simulation of the delta-sigma modulator.

the quantization noise is high-pass filtered, with the majority of the noise occurring at higher frequencies. If an oversampling ratio of 64 is assumed, then the SQNR is 82.03 dB, which corresponds to an effective resolution of 13.33 bits.

One question that remains is how to extract the high-resolution data from the low-resolution modulator output. For instance, the third-order modulator described above has a 1-bit output bitstream, but an effective resolution of over 13 bits. This conversion is accomplished by using a decimation filter. A decimation filter is a digital filter that performs two functions. First, it applies a low-pass filter to remove the spectral components that fall above the desired signal bandwidth while simultaneously increasing the width of the data to match the resolution of the full ADC. This filtering will remove the quantization noise that has been shaped to higher frequencies. Second, the decimation filter downsamples the data to the Nyquist sampling rate. Decimation filters for delta-sigma modulators are typically implemented with low-pass sinc filters where the order of the sinc filter is one higher than the order of the modulator loop filter [7].

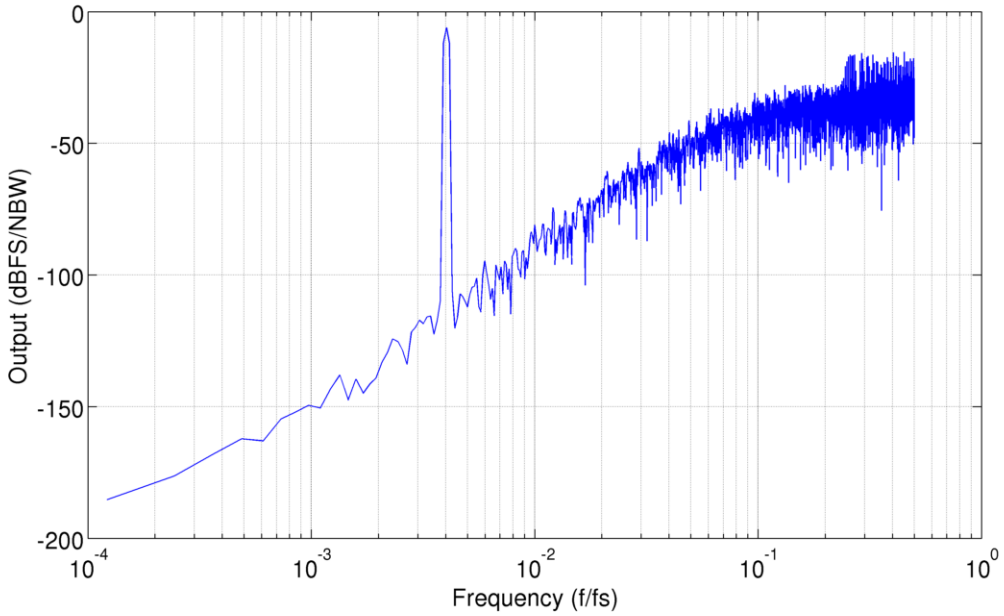


Figure 2.13: Output spectrum of the delta-sigma modulator.

2.2.4 Continuous-Time Delta-Sigma Modulators

Historically, the majority of delta-sigma modulators have been implemented with discrete-time loop filters. These filters are built with switched-capacitor circuits that exhibit good accuracy and linearity [26]. However, discrete-time modulators are limited in terms of their maximum speed and the requirement that sampling be performed at the input of the modulator. An alternative is to implement the modulator with a continuous-time loop filter.

Figure 2.14 shows the block diagram of a continuous-time delta-sigma modulator. There are two differences when comparing the continuous-time modulator with the discrete-time modulator shown in Figure 2.10. First, the discrete-time loop filter, $A(z)$, is replaced with a continuous-time loop filter, $A(s)$. Second, the input signal is now a continuous-time signal, while in the discrete-time modulator the input was a sampled signal.

There are two primary benefits of using a continuous-time loop filter in a delta-sigma modulator. The first is related to the speed of the modulator. In a discrete-time

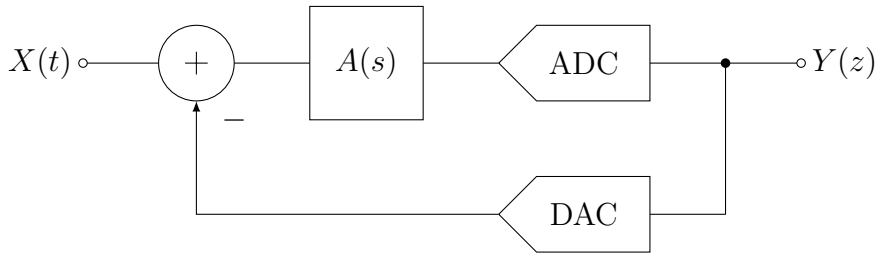


Figure 2.14: Block diagram of a continuous-time delta-sigma modulator.

modulator the signal is a series of fast changing pulses. The maximum clock rate of the modulator is therefore limited by the settling time of the integrators, which is determined by the bandwidth of the amplifiers used in the loop filter. In a continuous-time modulator the signals are continuous, which greatly reduces the requirements on the amplifiers. As a result, a continuous-time modulator can be clocked two to four times faster than an equivalent discrete-time modulator [45].

The second benefit is the implicit anti-alias filter [38]. In a discrete-time modulator the input signal must be sampled at the input of the modulator. This places stringent requirements on the sample and hold circuit and mandates the use of an anti-alias filter to prevent out of band signals from aliasing into the signal band. In a continuous-time modulator sampling doesn't occur until the signal reaches the internal ADC, which is after the loop filter. As a result, the continuous-time modulator has an implicit anti-alias filtering characteristic, which is easy to understand because the signal passes through the loop filter before being sampled. The implicit anti-alias filter response for a third-order single-bit continuous-time modulator is shown in Figure 2.15. The filter has a sinc characteristic with nulls at multiples of the sampling frequency. These nulls are conveniently located at frequencies that would alias into the signal band.

While these benefits make continuous-time modulators an attractive option, there are a few drawbacks to using them. The first is that they are more sensitive to clock jitter than their discrete-time counterparts [12]. This is because the feedback signal from the DAC is typically a constant current pulse that lasts for the duration of the clock period, which means that the total charge deposited on the capacitor used in

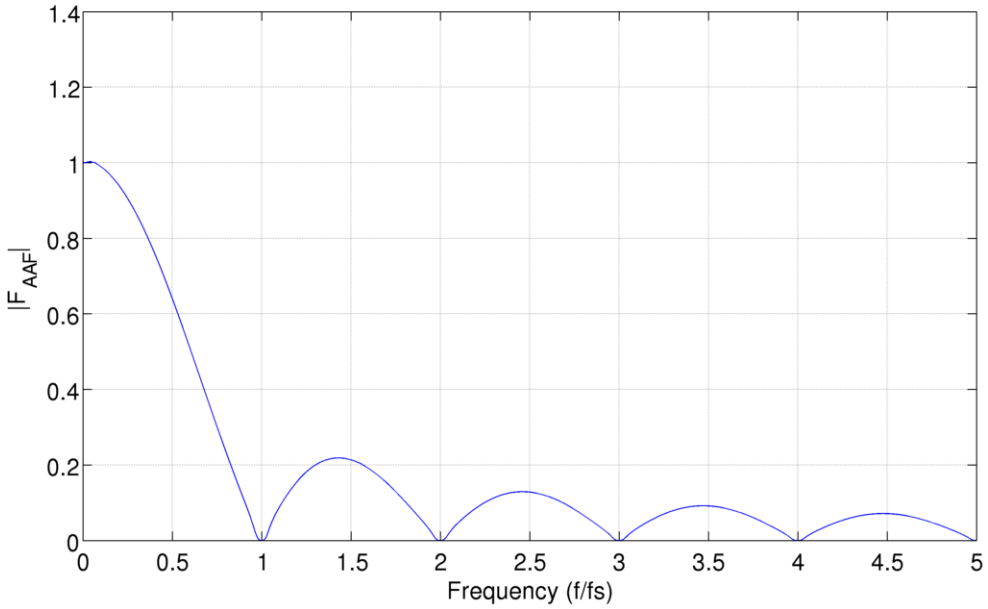


Figure 2.15: Response of the implicit anti-alias filter of a third-order continuous-time delta-sigma modulator.

the continuous-time integrator is

$$Q_{\mathrm{DAC}} = I_{\mathrm{DAC}} T_{\mathrm{s}} \tag{2.33}$$

where I_{DAC} is the DAC current and T_{s} is the sampling period. Any error in the clock period will result in a proportional error in the total feedback charge. The primary method to mitigate this problem is to use non-rectangular DAC pulse shapes, but this approach places additional strain on the amplifiers in the loop filter. Clock jitter becomes particularly problematic at high sampling rates, where the magnitude of the jitter is a significant fraction of the sampling period. At low sampling rates it can often be disregarded.

The other main issue that affects continuous-time modulators is excess loop delay [14]. In a discrete-time modulator the signals in the modulator only need to be valid at the sampling instants, which gives them a full clock period to settle to an

accurate value. As a result, a small amount of delay in the feedback path isn't problematic as long as there is enough settling time. In a continuous-time modulator the signals have to be valid at all times, so any delay causes inaccuracies. This delay could be caused by the finite decision time of the internal quantizer or the response time of the DAC. There are several methods to overcome this problem. If the amount of excess loop delay is fixed, then the loop filter coefficients can be adjusted to compensate for this delay. If the delay is signal dependent, which is often the case for quantizer delay, then a fixed delay can be added to the loop to give the quantizer additional decision time. The loop filter can then be modified to compensate for this fixed delay.

The design process for implementing a continuous-time delta-sigma modulator starts with the design of a discrete-time modulator. Due to the wide availability of design tools for discrete-time modulators, it is generally straightforward to design a discrete-time loop filter. From there, the discrete-time loop filter is converted into an equivalent continuous-time loop filter. The two primary methods for accomplishing this are the impulse-invariant transform and the modified z-transform [38]. The impulse-invariant transform attempts to find the continuous-time loop filter coefficients that result in an equivalent impulse response to the discrete-time loop filter. The modified z-transform computes the equivalent discrete-time loop filter from the continuous-time loop filter and then compares it with the original discrete-time loop filter to determine the coefficients. Both methods produce similar results in most cases.

In a continuous-time modulator there are many different circuit architectures that can be used to implement the integrators, each with its own benefits. Two of the most common are the active-RC integrator and the gm-C integrator. Active-RC integrators generally have the highest linearity at the expense the power consumption and tunability, while gm-C integrators generally have the highest speed and lowest power consumption at the expense of linearity. Other architectures include active gm-C integrators, active MOS-C integrators and log integrators. The choice of integrator architecture is application specific and often multiple integrator architectures are used in the same ADC design.

Chapter 3

Receiver Overview

3.1 Performance Metrics

Specialized receiver hardware is required to collect broadband VLF magnetic field data with the accuracy and resolution necessary for scientific research due to the unique nature of these signals [39]. To receive high quality data, an example of which was shown in the spectrogram in Figure 1.2, the receiver must have certain performance characteristics. The four most important performance characteristics for a VLF magnetic field receiver are described in this section. These include the receiver bandwidth, gain, sensitivity and spurious-free dynamic range. A detailed list that summarizes all of the design goals and specifications is given in Section 3.4.

3.1.1 Bandwidth

The first key specification is the receiver bandwidth, which is defined as the 3 dB cutoff from the low-end of the frequency band to the high-end of the frequency band. A flat frequency response is desired due to the roughly constant power spectral density of naturally occurring VLF signals. The goal for the receiver is to have a flat response that extends from 300 Hz to 50 kHz.

At the low-end of the frequency range the receiver response is limited by the impedance of the antenna. A standard 1 Ω, 1 mH antenna is used by all of the VLF

receivers deployed by the Stanford VLF group, so there is minimal control over the low frequency cutoff. At the high-end of the frequency range the bandwidth is limited by the bandwidth of the low-noise amplifier used in the receiver.

The goal for the high frequency cutoff of the receiver is 50 kHz, which is higher than the normal limit of the VLF band of 30 kHz. The reason for this extended bandwidth is because several signals of interest occur just above the standard 30 kHz VLF limit [18]. One example is the NAU transmitter in Puetro Rico that transmits at 40.75 kHz.

It is important to point out that a broadband VLF receiver is very different from a standard RF receiver. In a standard RF receiver a mixer is used to frequency shift a narrow-band signal from a high RF frequency to a low frequency where it can be digitized and processed. In contrast, in a broadband VLF receiver there is no frequency shifting because the signal is already at a low frequency. In this case, the entire VLF band can be directly digitized. Therefore, the bandwidth of the receiver must cover the entire VLF band.

3.1.2 Gain

The gain of the receiver is defined as the transimpedance gain (current-to-voltage) from the input of the receiver to the output of the receiver. The goal for the receiver is to have a transimpedance gain of approximately 100 dB. In terms of the received magnetic field, this amount of gain corresponds to 0.63 mV/pT when using a six-turn 4.9 meter square antenna. This is the standard antenna size for comparing receiver performance.

The large amount of transimpedance gain is necessary because naturally occurring VLF signals are often very small. As a result, a significant amount of gain is required to amplify the signals enough to be captured by the ADC. This amount of gain is consistent with previous VLF receiver designs deployed by the Stanford VLF research group when accounting for differences in the ADC full-scale range and supply voltage.

To support a variety of applications, the single-chip receiver described in this dissertation implements multiple gain levels. The single-chip receiver includes four gain

modes with transimpedance gain values of approximately 90 dB, 100 dB, 110 dB and 120 dB. This enables the user to select the appropriate amount of gain depending on the application and location of the receiver. For example, in a noisy urban environment the lower gain modes may be needed to prevent the receiver from saturating. On the other hand, in a remote area with little noise the higher gain modes could be used to further amplify the small VLF signals.

3.1.3 Sensitivity

The sensitivity of the receiver is defined as the magnetic field amplitude at the antenna that results in a 0 dB signal-to-noise ratio at the output of the receiver when calculated in a 1 Hz bandwidth [39]. Essentially, the sensitivity is the minimum detectable signal. It is a signal with an amplitude that is ultimately equal to the output noise floor of the receiver. A smaller sensitivity is better. The desired sensitivity of the receiver is below 1 $\mathrm{fT/Hz^{1/2}}$ over the entire receiver bandwidth, which is from 300 Hz to 50 kHz.

The target sensitivity is 1 $\mathrm{fT/Hz^{1/2}}$ because the environmental noise in the VLF band is between 1 $\mathrm{fT/Hz^{1/2}}$ and 2 $\mathrm{fT/Hz^{1/2}}$ at the quietest locations [15]. Designing the receiver to have a sensitivity below the environmental noise floor ensures that the noise contributed by the receiver does not degrade the received data.

It is important to note that the sensitivity of the receiver depends on the size of the antenna. For the purposes of design and testing, a six-turn 4.9 meter square antenna is assumed. A larger antenna will result in better sensitivity, while a smaller antenna will result in worse sensitivity. The size of the antenna deployed will depend on the desired sensitivity, as well as the amount of expected interference at the receiver site.

3.1.4 Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is a measure of the linearity of the receiver. When a sinusoidal signal is applied to the input of the receiver, the SFDR is defined as the ratio of the magnitude of the input tone to the magnitude of the largest spurious tone in the output spectrum of the receiver [38]. Typically the largest spurious tone is a harmonic of the input signal. An example of the SFDR calculation is shown in

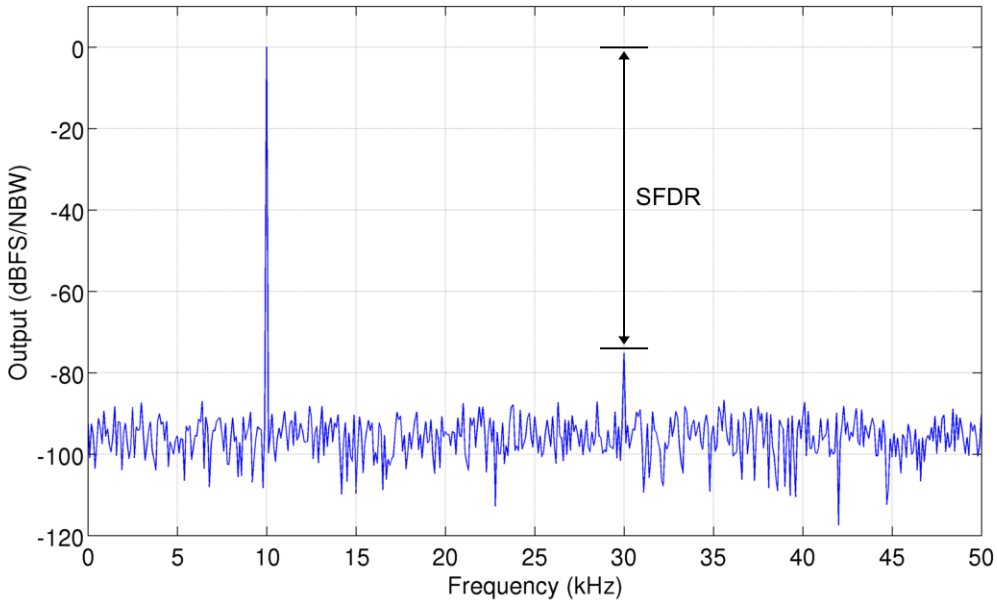


Figure 3.1: Example of the calculation of the spurious-free dynamic range.

Figure 3.1. This example shows an output spectrum with a 10 kHz sinusoidal input signal. The largest spurious tone is the third harmonic at 30 kHz. Therefore, in this example the SFDR is the difference between the fundamental and the third harmonic, which is 75 dB.

The goal for the SFDR is 90 dB at all frequencies in the receiver bandwidth. A large SFDR is necessary because strong transmitters, as well as weak naturally occurring VLF signals, fall within the VLF band. Poor linearity would result in the harmonic distortion from the strong transmitters corrupting the smaller signals. The difference between the largest transmitters and the smallest VLF signals can be as large as 90 dB.

3.2 Existing VLF Receivers

Over the past several decades the Stanford VLF research group has deployed many different VLF receivers. The two most recent and widely used are discussed in this section. The first is the AWESOME receiver, which is the high-performance receiver

currently deployed around the world. The second is the Penguin receiver, which is the low-power receiver that is used for remote deployments.

3.2.1 AWESOME Receiver

The primary receiver used by the Stanford VLF research group is the AWESOME receiver [19]. AWESOME is an acronym which stands for Atmospheric Weather Electromagnetic System for Observation, Modeling and Education. The AWESOME receiver is deployed around the world in locations including Japan, Australia, Hawaii, Europe and Africa. The global network of receivers constantly collects, processes and stores the VLF data that is received. In some cases the data is automatically uploaded to servers at Stanford for further analysis.

The AWESOME receiver is the gold-standard VLF receiver. It has the highest data quality of any of the VLF receivers developed at Stanford. It is a broadband receiver that covers the entire VLF range from approximately 300 Hz to 50 kHz. It has a sensitivity of around 1 $\mathrm{fT/Hz^{1/2}}$ and a spurious-free dynamic range of approximately 90 dB. Due to its high data quality, the AWESOME receiver is often used as a benchmark to compare new receiver designs.

Despite its good performance, the AWESOME receiver has several weaknesses that prevent it from being used in some applications. The first is its power consumption. The signal path power consumption of the receiver is approximately 10 Watts. Additional power is consumed by support circuitry, which includes a GPS time reference, calibration circuitry and digital communication interfaces. The receiver also requires a computer, either a desktop or a laptop, to process and store the received data. The total power consumption of the AWESOME receiver is around 60 W when combined with a low power laptop. A typical implementation uses a standard desktop computer, which likely pushes the total power dissipation over 200 W. The high power dissipation prevents the AWESOME receiver from being used in remote locations where it would be required to operate on battery power for long periods of time.

The other weakness of the AWESOME receiver is its size. The receiver consists of

two metal enclosures. One enclosure contains the digital portion of the receiver and the other holds the analog components. Each enclosure is approximately 12 inches wide by 12 inches long by 8 inches tall. This does not include the size of the desktop or laptop computer. The large size would preclude the AWESOME receiver from use in a mobile or hand-held application.

3.2.2 Penguin Receiver

The Penguin receiver is a broadband VLF receiver that is designed for remote deployments [32]. Penguin is an acronym which stands for Polar Experiment Network for Geophysical Upper-atmosphere Investigations. The Penguin receiver is deployed in remote locations where AC power is not available. The receiver is optimized for low power dissipation and can run on battery power for long periods of time. It uses a custom designed low-noise amplifier ASIC that was also developed by the Stanford VLF research group [28]. The receiver is designed to have enough data storage and battery power to run autonomously for up to one year without maintenance. The Penguin receiver was successfully deployed in Antarctica at Amundsen-Scott South Pole Station in 2009.

The signal path power consumption of the Penguin receiver is approximately 50 mW, which is considerably less than that of the AWESOME receiver. Additional power is consumed by support circuitry, but the Penguin receiver does not require a separate desktop or laptop computer. The data quality of the Penguin receiver is not as good as the AWESOME receiver's data quality. While both receivers have a sensitivity of approximately 1 $\mathrm{fT/Hz^{1/2}}$, the Penguin receiver has a maximum signal frequency of 30 kHz and a spurious-free dynamic range of roughly 65 dB. The size of the Penguin receiver is similar to that of the AWESOME receiver. It consists of two metal enclosures with dimensions of approximately 12 inches wide by 12 inches long by 8 inches tall.

One issue that was uncovered after the deployment of the Penguin receiver was its sensitivity to temperature variations. Namely, it was discovered that the biasing of the low-noise amplifier was not robust to large temperature swings. As a result, the

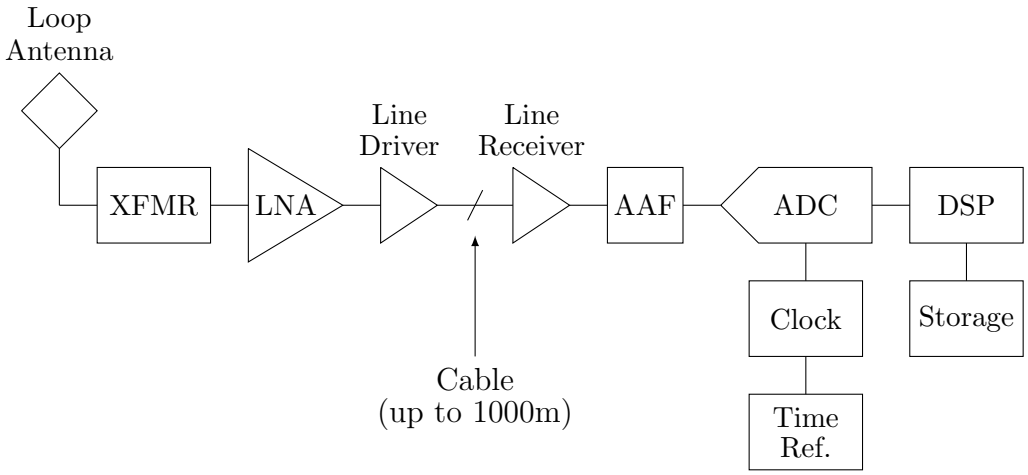


Figure 3.2: Block diagram of the traditional receiver architecture.

noise performance of the receiver was reduced if the temperature changed significantly because the biasing could only be optimized for one specific temperature.

3.3 Receiver Architecture

3.3.1 Traditional Architecture

The AWESOME receiver and the Penguin receiver, as well as previous VLF magnetic field receivers designed by the Stanford VLF group, use a similar receiver architecture. Figure 3.2 shows this traditional receiver architecture. While this discussion focuses on a magnetic field receiver architecture, a similar architecture has been used for an electric field receiver [37]. The traditional magnetic field receiver architecture is divided into two sections: the analog front-end and the digital back-end.

The magnetic field antenna is a loop antenna. The size of the loop and the number of turns can vary depending on the desired receiver sensitivity and the amount of interference at the receiver location. All of the antennas have a 1 Ω, 1 mH impedance so that different antennas can be used interchangeably with the same receiver. The constant antenna impedance also ensures that different receiver designs can be used with the same antenna.

The antenna connects directly to the analog front-end. The analog front-end consists of a transformer, a low-noise amplifier and a line driver. The transformer is used to reduce the resistance looking into the receiver in order to ensure a low input turnover frequency. Ideally the input resistance is much less than the resistance of the antenna, but for practical considerations it is often set equal to the antenna resistance of 1 Ω. The standard transformer is a 24:548 turns ratio hand-wound center-tapped transformer. After the transformer, a low-noise amplifier (LNA) is employed to increase the amplitude of the received signal while adding as little noise as possible. The signal then passes through a line driver circuit, which further amplifies the signal and drives a low impedance cable that connects the analog front-end to the digital back-end.

The signal from the analog front-end is processed by the digital back-end, which consists of a line receiver, an anti-alias filter (AAF), an analog-to-digital converter (ADC), as well as several auxiliary components. The line receiver terminates the cable from the analog front-end and provides any additional gain that is needed to match the signal swing to the full scale range of the ADC. An anti-alias filter follows the line receiver and provides a sharp low-pass filter with a cut-off frequency that falls just above the receiver bandwidth. The AAF can be implemented with an active circuit or a passive filter and is necessary to prevent aliasing caused by the sampling operation of the ADC. Finally, the ADC converts the analog signal into digital values for further processing and storage.

The digital back-end includes several additional subsystems that perform functions outside the signal path of the receiver. These systems include the time reference, clock generator, digital signal processing and data storage. The time reference is particularly important and is typically implemented with a GPS receiver and additional logic that uses the one pulse per second GPS signal to ensure an accurate sampling frequency [17]. Accurate sampling is necessary for interferometric measurements in which a VLF event is captured simultaneously at multiple receiver locations and precise timestamps are needed to compare the data. The time reference includes a feedback system which adjusts the frequency of the clock generator based on the one pulse per second GPS signal. This compensates for inaccuracies in the clock

generator frequency. Depending on the application and the accuracy of the clock generator, the time reference may correct the clock frequency every second or only periodically.

Additionally, the digital back-end includes digital-signal processing (DSP) and data storage. The DSP may provide real-time spectral analysis or data compression. It may also be used to implement the digital interfaces with the data storage system. The type of data storage is application specific. For example, in the AWESOME receiver an external hard-drive connected to a computer is used for storage. In the Penguin receiver a CompactFlash card is used to eliminate the need for a computer.

The analog front-end and the digital back-end are often separated by a long cable. The enclosure that holds the analog front-end is typically placed very close to the antenna to prevent resistive losses in the wires. The digital back-end is placed indoors where it can be near a computer and a source of AC power. The primary reason for having a long cable between the analog front-end and the digital back-end is to prevent the antenna from picking up any interference radiated by the potentially noisy digital circuits. This also allows for the antenna to be placed a long distance from any other sources of noise, such as power lines or other electronic equipment. Typically a 100 Ω cable is used and separation distances of up to 1000 meters have been successfully deployed. Due to its low-power design and self-contained data storage, the Penguin receiver has minimal radiated interference. As a result, it is not strictly necessary to separate the digital and analog portions of the Penguin receiver. However, the analog front-end and the digital back-end are still placed in separate enclosures with a cable between them for legacy reasons.

3.3.2 Single-Chip Architecture

The single-chip VLF magnetic field receiver presented in this dissertation uses an optimized receiver architecture. Figure 3.3 shows the single-chip receiver architecture. The signal path of the receiver consists of a loop antenna, transformer, LNA and ADC. The architecture also includes the same auxiliary subsystems seen in the traditional receiver architecture, including the time reference, clock generator, digital

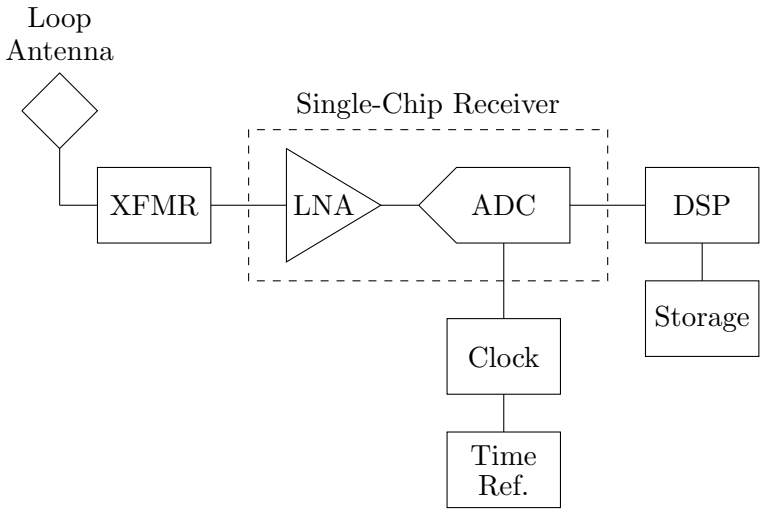


Figure 3.3: Block diagram of the single-chip receiver architecture

signal processing and data storage.

The loop antenna in the single-chip receiver architecture is a 1 Ω, 1 mH antenna that is identical to the one used by both the AWESOME receiver and Penguin receiver. This ensures compatibility with already installed antennas. Similarly, the receiver uses the same 24:548 center-tapped transformer for impedance matching the antenna to the input of the receiver. The single-chip receiver uses a low-noise amplifier at its input, followed immediately by an analog-to-digital converter.

There are two key differences between the single-chip architecture and the traditional architecture. The first is that the single-chip architecture does not include an explicit anti-alias filter (AAF). The AAF prevents signals from aliasing into the signal band as a result of the sampling operation performed by the ADC. The AAF is eliminated by using an ADC architecture that does not require an AAF. Eliminating the AAF results in a significant power savings. In the Penguin receiver, for example, the AAF uses approximately 40% of the total signal path power consumption. In addition to burning a large amount of power, the AAF can be challenging to design as it can degrade the linearity of the receiver.

The second primary difference is that the single-chip architecture does not separate the analog front-end from the digital back-end with a long cable. This simplifies the

architecture as the line driver and line receiver are no longer necessary. This is possible because the single-chip receiver targets low power applications. As a result, all of the circuits run on battery power and exhibit minimal radiated interference.

The goal of this work is to integrate the entire signal path of the receiver on a single chip. The signal path includes the low-noise amplifier and the analog-to-digital converter, as highlighted in Figure 3.3. The auxiliary subsystems, such as the time reference and digital signal processing, are not included on-chip as they are application specific.

There are three primary benefits to implementing the receiver on a single chip. The first is that it reduces the size of the receiver. Significantly reducing the size opens up new applications, such as the possibility of a hand-held VLF receiver. The second benefit is reduced cost. The AWESOME receiver, for example, costs approximately $3,000. A fabrication run of the single-chip receiver would result in thousands of chips with a unit cost orders of magnitude less than the cost of an AWESOME receiver. The third benefit is simplicity. Currently, deploying a VLF receiver requires detailed knowledge of the various receiver components. A single-chip receiver would simplify the deployment process by requiring only a single component. The single-chip receiver would interface with the antenna, produce digital output data and guarantee a certain level of performance. While a single-chip implementation of a VLF receiver provides a number of benefits, it also presents design challenges. The most critical challenge is noise coupling between the potentially noisy digital circuits in the ADC and the sensitive analog circuits in the LNA, which both reside on the same die.

3.4 Design Specifications

The goal for the single-chip VLF magnetic field receiver is to achieve the high data quality of the AWESOME receiver while having a low power dissipation similar to that of the Penguin receiver. The full design specifications are summarized in Table 3.1. The objective is to achieve the design specifications while minimizing the power dissipation. The specifications can be broken down into the various components of the design, which include the low-noise amplifier, the analog-to-digital converter, the full

Table 3.1: Design specifications for the single-chip receiver.

Component	Specification	Goal
Low-Noise Amplifier	Bandwidth	300 Hz to 50 kHz
	Gain	100 dB
	Sensitivity	1 fT/Hz$^{1/2}$
	SFDR	90 dB
Analog-to-Digital Converter	Bandwidth	50 kHz
	Resolution	12 bits
	SFDR	90 dB
Receiver	Alias Rejection	80 dB
	Temperature	$-70°$ C to $125°$ C
	Antenna	1 Ω / 1 mH
	Transformer	24:548 CT
Technology	Process	0.13 µm BiCMOS
	Supply Voltage	1.2 V

receiver and the implementation technology.

The design goals for the LNA follow directly from the key performance metrics described in Section 3.1. The bandwidth of the LNA must extend from 300 Hz to 50 kHz with a flat frequency response over this range. The transimpedance gain of the receiver needs to be approximately 100 dB. To achieve this goal, the single-chip receiver implements multiple gain modes that span a range of 90 dB to 120 dB. The sensitivity of the receiver needs to be less than 1 fT/Hz$^{1/2}$ and the spurious-free dynamic range should be at least 90 dB.

The goal for the ADC is to digitize the received signal without degrading the quality of the data. The ADC requires a bandwidth of 50 kHz to capture the full VLF band and a spurious-free dynamic range of 90 dB. Previous work by the Stanford VLF research group has shown that in order to achieve 90 dB SFDR, a resolution of at least 10 bits is necessary given the desired frequency resolution of the output spectrum [49]. To achieve the SFDR goal and to ensure that the noise from the ADC is negligible compared to the LNA, the target resolution for the ADC is 12 bits.

In addition to the design goals for the LNA and ADC, there are also specifications

for the receiver as a whole. The first is related to aliasing. Although the single-chip receiver architecture does not include an explicit anti-alias filter, the receiver still requires at least 80 dB of alias suppression to prevent out of band signals from aliasing into the VLF band and corrupting the received data. The receiver also must be able to operate over a wide range of temperatures, which extends from -70° C to 125° C, to account for the conditions at the remote deployment locations. As discussed previously, the single-chip receiver is designed to use the standard 1 Ω, 1 mH loop antenna and the standard 24:548 center-tapped transformer. In terms of implementing the integrated circuit, the single-chip receiver uses a 0.13 µm BiCMOS process, which has a nominal supply voltage of 1.2 V.

Chapter 4

Circuit Implementation

This chapter covers the circuit implementation of the single-chip VLF magnetic field receiver. The primary challenge in the design of the receiver is achieving the high level of performance outlined in Section 3.4, while minimizing the power dissipation. To reduce the power dissipation, the receiver uses a 1.2 V supply voltage. As a result, low-voltage design techniques are required to achieve the performance goals with reduced headroom [51]. To further complicate the design, the receiver is required to be capable of operating in remote environments, such as at the South Pole where temperatures can be below -70° C in the winter [47]. To overcome this challenge, steps are taken in the design of the receiver to ensure that it can operate properly over the wide range of conditions that may be encountered in the field.

This chapter is divided into five parts. The first part covers the design of the low-noise amplifier (LNA). This section includes an overview of the LNA architecture and the design details for the input stage, gain stage and automatic biasing circuits. The second part covers the design of the analog-to-digital converter (ADC). This part includes the top-level design of the continuous-time delta-sigma modulator and the transistor-level design of the RC integrator stages, the comparator, the flipflop and the feedback digital-to-analog converters (DACs). The third part covers the design of the two-stage Miller compensated operational transconductance amplifier (OTA), which is used throughout the LNA and ADC. The fourth part covers the design of the full receiver, which includes the top-level architecture and the strategies employed to

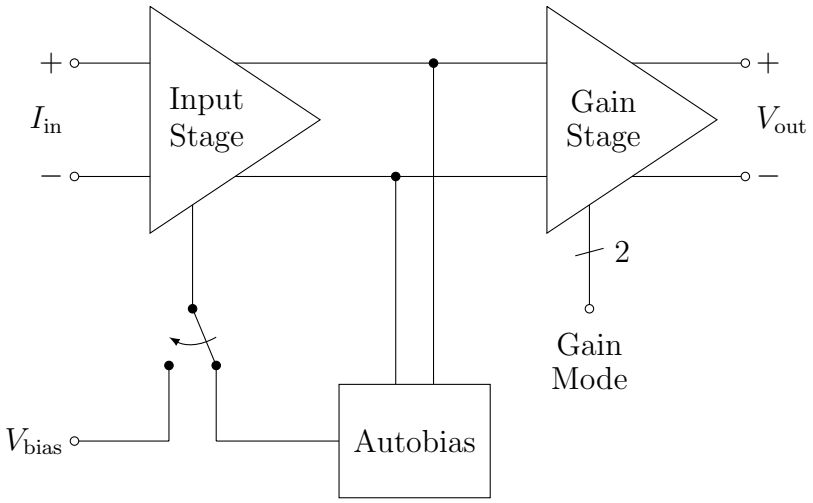


Figure 4.1: Top-level block diagram of the LNA.

reduce noise coupling between the LNA and ADC. Finally, the fifth part details the layout of the test chip.

4.1 LNA Implementation

4.1.1 Overview

The top-level architecture of the LNA is shown in Figure 4.1. The LNA is a two-stage amplifier. The first amplifier stage, the input stage, is a transimpedance amplifier that converts the input signal from a current to a voltage. The input stage also provides a low input impedance to properly match the antenna and provide an optimal receiver frequency response. According to Frii's formula for noise, the first stage of a multi-stage amplifier contributes the most noise to the system assuming that subsequent stages provide considerable gain [22]. As a result, the noise performance is a primary design consideration for the LNA input stage to ensure good overall receiver sensitivity.

The second amplifier stage, the gain stage, is a variable-gain voltage amplifier with four discrete gain modes. The gain stage produces the final output of the LNA, which means that its output will experience the largest voltage swings. For this reason, the

linearity of the gain stage is a primary concern in order to meet the spurious-free dynamic range design goal. Noise is also a consideration, but it is not as critical as in the input stage. The gain stage has four discrete gain modes, where the gain mode is selected by a two-bit digital signal that is controlled external to the chip. A standard decoder with NAND logic is used to convert the two-bit digital signal into four one-hot control lines.

A bias voltage is required to set the DC current in the input stage. There are two methods to set this bias voltage. The first is with an external voltage that is set outside the test chip. This voltage could be set with a potentiometer or provided by a DC power supply. While this method may be useful for basic testing, it can run into problems in the field due to temperature variations and component drift. To overcome these problems, a second method to set the input stage bias voltage is included. The second method is an automatic biasing circuit, which is more robust. This method uses a feedback circuit to automatically set the optimal bias voltage regardless of temperature changes or component drift. An external control signal is used to select the biasing mode using an analog multiplexer that consists of two CMOS transmission gates.

4.1.2 Input Stage

There are several competing goals in the design of the LNA input stage. The input stage must provide a large transimpedance gain (current-to-voltage) while adding as little noise as possible to the signal to ensure good receiver sensitivity. It also needs to have a low input impedance to avoid adversely affecting the input turnover frequency, which is the frequency above which the receiver response is flat. Finally, the input stage must not degrade the linearity of the receiver or have a large offset voltage.

A number of different amplifier architectures could be used in the input stage, each with different performance characteristics. For example, previous work has explored using a resistor to terminate the antenna followed by a voltage amplifier. However, this architecture does not have optimal noise performance. Another idea might be to use a voltage amplifier with feedback to reduce the input impedance, but stability

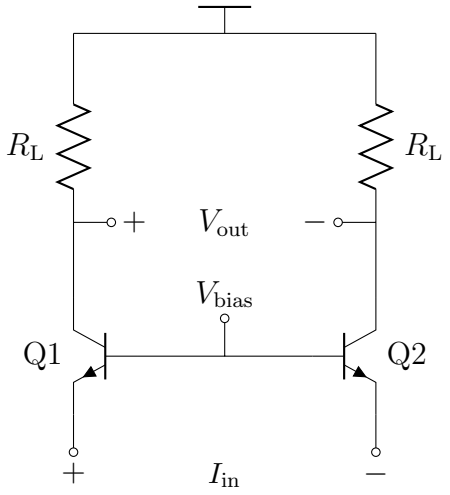


Figure 4.2: Schematic of the common-base input stage.

problems are encountered. A thorough analysis of the different architectures revealed that a low-impedance amplifier produces the best overall performance [39]. For this reason, a differential bipolar common-base amplifier is selected.

A common-gate amplifier, the CMOS equivalent, would also be suitable for this application. However, the bipolar implementation was selected for two reasons. First, the flicker noise ($1/f$ noise) performance of the bipolar transistors was superior in the target process. Second, bipolar transistors have better current efficiency, meaning that they can generate the same transconductance with lower bias current. The better current efficiency translates to an input stage that uses less power for equivalent performance.

The common-base input stage is shown in Figure 4.2. The amplifier consists of two bipolar transistors, Q1 and Q2. The collectors of the two transistors are each connected to a load resistor, R_{L}. The emitters serve as the differential input port and the base is connected to a DC bias voltage.

The gain of the input stage can be calculated by considering the differential half-circuit and applying small-signal analysis. The transimpedance gain, which is the ratio of the output voltage to the input current, is

$$A_{\mathrm{Z}} = \frac{V_{\mathrm{out}}}{I_{\mathrm{in}}} = \alpha R_{\mathrm{L}} \tag{4.1}$$

where

$$\alpha = \frac{\beta}{1+\beta} \tag{4.2}$$

Typical β values for NPN transistors in integrated circuits range from 50 to 500, which means that α is approximately one [25]. Therefore, the transimpedance gain of the input stage can be approximated as R_{L}, the value of the load resistor. This result makes sense, because under ideal conditions the current gain of a common-base amplifier is one.

The input impedance of the input stage of the LNA directly affects the frequency response of the receiver. Recall from Section 2.1.2 that the input turnover frequency is

$$f_{\mathrm{i}} = \frac{R_{\mathrm{a}} + R_{\mathrm{in}}/m^2}{2\pi L_{\mathrm{a}}} \tag{4.3}$$

At frequencies below f_{i}, the magnitude of the receiver output is proportional to frequency. At frequencies above f_{i}, the output is flat with frequency. Ideally R_{in}/m^2 would be zero to minimize the input turnover frequency, maximizing the flat region of the frequency response. However, this is not practical, so typically the input impedance is set such that $R_{\mathrm{in}}/m^2 \approx R_{\mathrm{a}}$. With a standard 1 Ω, 1 mH antenna and the 24:548 transformer ($m = 22.83$), this gives an input turnover frequency of approximately 318 Hz, which matches up nicely with the start of the VLF band (300 Hz).

The input impedance of the differential common-base amplifier can be calculated using small-signal analysis, resulting in

$$R_{\mathrm{in}} = \frac{2}{g_{\mathrm{m}} + \frac{1}{r_\pi}} \tag{4.4}$$

The factor of two is due to the fact that the amplifier is differential. Assuming that the β of the transistor is much greater than one, then r_π is large and the input impedance simplifies to

$$R_{\mathrm{in}} = \frac{2}{g_{\mathrm{m}}} \tag{4.5}$$

This result shows that the input impedance depends primarily on the transconductance of the NPN transistors, which in turn depends on the bias current because

$g_{\mathrm{m}} = I_{\mathrm{C}}/V_{\mathrm{T}}$. Increasing the current will decrease the input impedance, while decreasing the current will increase the input impedance. To satisfy $R_{\mathrm{in}}/m^2 \approx R_{\mathrm{a}}$, the bias current in each side of the amplifier is set to 100 µA.

The noise performance of the input stage is critical to the sensitivity of the receiver. This is because, according to Frii's formula for noise, the first amplifying stage of a receiver primarily sets the noise performance of the full receiver. The noise performance of the common-base input stage can be analyzed by adding the relevant noise sources. Figure 4.3 shows the differential half-circuit with the noise sources added. The load resistor contributes mean-square thermal noise of

$$\overline{i_{\mathrm{L}}^2} = 4kT\frac{1}{R_{\mathrm{L}}}\Delta f \tag{4.6}$$

where k is the Boltzmann constant, T is the temperature and Δf is the bandwidth over which the noise is being calculated [25]. The bipolar transistor contributes shot noise and flicker noise through two noise sources with mean-square values of

$$\overline{i_{\mathrm{c}}^2} = 2qI_{\mathrm{C}}\Delta f \tag{4.7}$$

$$\overline{i_{\mathrm{b}}^2} = 2qI_{\mathrm{B}}\Delta f + K_1\frac{I_{\mathrm{B}}^a}{f}\Delta f \tag{4.8}$$

where I_{C} is the collector current, I_{B} is the base current, q is the charge of an electron (1.6×10^{-19}), and K_1 and a are constants that capture the $1/f$ noise characteristics of a particular device [25].

To analyze the effect of these noise sources on the sensitivity of the receiver, the noise sources can be referred to the input of the amplifier. This process results in an input voltage noise source and input current noise source that are equivalent to the internal noise sources of the amplifier. The input referred mean-square noise sources are

$$\overline{v_{\mathrm{i}}^2} = 4kT\left(r_{\mathrm{b}} + \frac{1}{2g_{\mathrm{m}}}\right)\Delta f \tag{4.9}$$

$$\overline{i_{\mathrm{i}}^2} = 2q\left(I_{\mathrm{B}} + K_1\frac{I_{\mathrm{B}}^a}{f} + \frac{I_{\mathrm{C}}}{\beta(j\omega)^2}\right)\Delta f + 4kT\frac{1}{R_{\mathrm{L}}}\Delta f \tag{4.10}$$

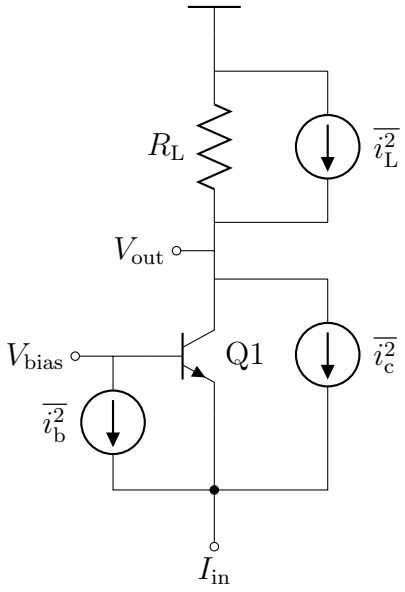


Figure 4.3: Simplified schematic of the input stage for noise analysis.

Notice that the noise from the load resistor is unattenuated when referred to the input. This is due to the fact that the current gain of the amplifier is one.

The receiver sensitivity depends on the noise from the antenna and the input referred noise from the LNA. Recall, from Section 2.1.2, that the receiver sensitivity can be expressed as

$$S_{\mathrm{sys}} = \frac{1}{\omega N A}\sqrt{\overline{v_{\mathrm{a}}^2} + \frac{\overline{v_{\mathrm{i}}^2}}{m^2} + \overline{i_{\mathrm{i}}^2} m^2 Z_{\mathrm{a}}^2} \tag{4.11}$$

In this expression the voltage noise terms are dominant at low frequencies, while the input referred current noise dominates in the receiver bandwidth because the antenna impedance Z_{a} increases with increasing frequency.

As a result, there are several design insights that can be gained from the input referred current noise expression in Equation 4.10. First, the load resistance should be made as large as possible to reduce its contribution to the noise. Second, the bias current should be as small as possible to reduce the noise from the NPN transistor. Both of these insights are consistent with other goals for the input stage. For example, the resistor is already set to the maximum possible value to give the maximum gain while still providing a suitable DC output voltage. Similarly, the bias current

is already set to the minimum value that produces the required input impedance. Finally, the $1/f$ noise is made negligible by using physically large NPN devices. This is accomplished by using many identical transistors connected in parallel.

Offset is another important design criteria for the input stage. This is because any offset is amplified by subsequent stages of the LNA, which could potentially degrade the performance of the receiver. Offset is caused by mismatch between components that are nominally identical. For example, the load resistors in the input stage are both designed to have the value R_{L}. However, random variations in the fabrication process will cause these resistors to not be exactly identical. Slightly different load resistor values will lead to slightly different DC output voltages for the two halves of the differential circuit. Mismatch between two components can be calculated with

$$\sigma_{\Delta \mathrm{X}} = \frac{A_{\mathrm{X}}}{\sqrt{WL}} \tag{4.12}$$

where $\sigma_{\Delta \mathrm{X}}$ is the standard deviation of the mismatch between two nearby components, A_{X} is a constant that characterizes the mismatch of a particular feature of the device, and W and L represent the width and length of the device [41].

To reduce the offset to an acceptable level, large areas are used for the both the NPN transistors and the load resistors. For the transistors, many unit sized devices are connected in parallel to increase the effective area. For the resistors, a large width is used to increase the total resistor area. Using large devices also helps reduce flicker noise, which is also inversely related to the device area.

The distortion of the input stage is another design consideration. However, since the signals at the output of the input stage are small compared to the signals in the subsequent stages of the LNA, it is expected that any distortion is minor. At any rate, the transimpedance gain of the input stage is simply R_{L}, which means that the linearity depends primarily on the linearity of the load resistor itself. There are several different types of resistors that can be built on integrated circuits. For this design, a high resistivity polysilicon resistor was used because it offered the best linearity when compared with the diffused resistors and well resistors in the target process.

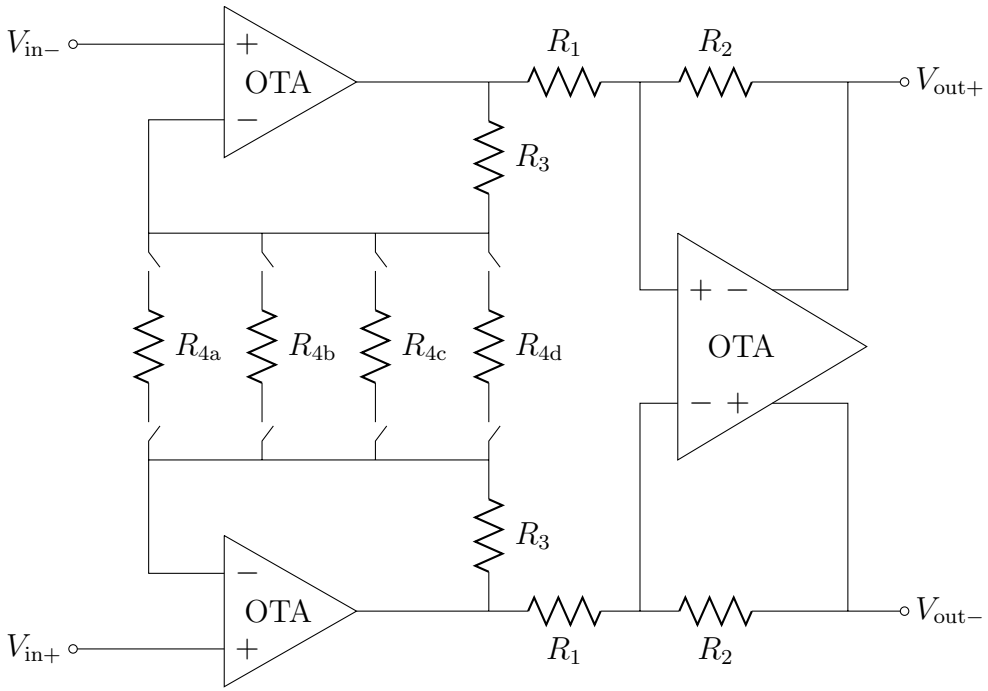


Figure 4.4: Schematic of the gain stage, which is implemented with a fully-differential instrumentation amplifier.

4.1.3 Gain Stage

The goal for the gain stage is to provide variable voltage gain while contributing as little noise and distortion as possible to the receiver. The gain stage must also provide a large input impedance to prevent loading the input stage. The gain stage is implemented with a fully-differential adaptation of an instrumentation amplifier [9]. An instrumentation amplifier is a common OPAMP circuit that is known for having a large input impedance, low noise and low distortion. The architecture for the gain stage is shown in Figure 4.4. The circuit consists of three operational transconductance amplifiers (OTAs) and a resistive network that sets the gain. The gain stage has fully-differential input and output ports. A switch network is used to select the R_4 resistor from a set of four possible values, which implements the four gain modes.

The gain of the gain stage can be divided into two parts. The first half consists of the two input OTAs, resistor R_3 and switchable resistor R_4. The gain of the first

half is

$$A_{\mathrm{v1}} = \left(1 + \frac{2R_3}{R_4}\right) \tag{4.13}$$

The values of the switchable resistor R_4 are chosen to implement 10 dB gain steps. Small values of R_4 give large gain, while large values of R_4 give small gain. The second half of the gain stage consists of the output OTA and resistors R_1 and R_2. The second half has a gain of

$$A_{\mathrm{v2}} = \frac{R_2}{R_1} \tag{4.14}$$

Combining these equations gives a total gain for the gain stage of

$$A_{\mathrm{v}} = A_{\mathrm{v1}}A_{\mathrm{v2}} = \frac{R_2}{R_1}\left(1 + \frac{2R_3}{R_4}\right) \tag{4.15}$$

The total gain of the gain stage is selected to give the appropriate range of gain values when combined with the gain of the input stage.

The input impedance of the gain stage is large because the differential input port is connected directly to the input of the OTAs. The CMOS transistors in the input differential pair of the OTA provide a capacitive impedance, which won't adversely affect the input stage.

The noise performance of the gain stage is important. It must be designed such that any noise contribution is small when referred back to the input of the receiver. The noise from the gain stage can be represented by an equivalent noise voltage and noise current at the input of the gain stage, $\overline{v_{\mathrm{i,GS}}^2}$ and $\overline{i_{\mathrm{i,GS}}^2}$ respectively. Referring these quantities to an effective noise current at the input of the receiver results in

$$\overline{i_{\mathrm{i}}^2} = \overline{i_{\mathrm{i,GS}}^2} + \frac{\overline{v_{\mathrm{i,GS}}^2}}{R_{\mathrm{L}}^2} \tag{4.16}$$

Notice that the gain stage current noise is unattenuated when referred to the input of the receiver. This is because the current gain of the input stage is one. As a result, the current noise of the gain stage is particularly important. On the other hand, the voltage noise is reduced by the gain of the input stage, which relaxes its design requirement.

The equivalent voltage noise and current noise sources at the input of the gain stage depend on the noise from the OTAs and the noise from the resistors. The equivalent noise sources are

$$\overline{v_{\mathrm{i,GS}}^2} = \overline{v_{\mathrm{i,OTA}}^2} + \overline{i_{\mathrm{i,OTA}}^2}\left(R_3 \parallel \frac{R_4}{2}\right) + 4kT\left(R_3 \parallel \frac{R_4}{2}\right)\Delta f \tag{4.17}$$

$$\overline{i_{\mathrm{i,GS}}^2} = \overline{i_{\mathrm{i,OTA}}^2} \tag{4.18}$$

where $\overline{v_{\mathrm{i,OTA}}^2}$ is the voltage noise from the OTA and $\overline{i_{\mathrm{i,OTA}}^2}$ is the current noise from the OTA. These expressions show that the current noise of the OTA must be minimized because it determines the current noise of the whole gain stage. Similarly, to reduce the voltage noise, steps must be taken to keep the OTA voltage noise small and the resistor values must be kept small. The dependence of the voltage noise on the resistor values will lead to slightly different noise levels in each of the gain modes. The highest gain mode (small R_4) will have the best noise performance, while the lowest gain mode (large R_4) will have the worst noise performance.

A two-stage CMOS architecture is used in the design of the OTAs. The equivalent noise sources for the OTA are

$$\overline{v_{\mathrm{i,OTA}}^2} = 8kT\frac{\gamma_{\mathrm{p}}}{g_{\mathrm{m1}}}\left(1 + \frac{\gamma_{\mathrm{n}}}{\gamma_{\mathrm{p}}}\frac{g_{\mathrm{m3}}}{g_{\mathrm{m1}}}\right)\Delta f \tag{4.19}$$

$$\overline{i_{\mathrm{i,OTA}}^2} = 2qI_{\mathrm{G}}\Delta f + 4kT\omega^2 C_{\mathrm{gs}}^2\frac{\gamma_{\mathrm{p}}}{g_{\mathrm{m1}}}\left(1 + \frac{\gamma_{\mathrm{n}}}{\gamma_{\mathrm{p}}}\frac{g_{\mathrm{m3}}}{g_{\mathrm{m1}}}\right)\Delta f \tag{4.20}$$

where γ_{p} is a coefficient that characterizes the noise of the PMOS transistors, γ_{n} is a coefficient that characterizes the noise of the NMOS transistors, g_{m1} is the transconductance of the input differential pair, g_{m3} is the transconductance of input stage load transistors, and I_{G} is the gate current of the input differential pair transistors. The CMOS architecture was chosen specifically for its good current noise performance, as shown in Equation 4.20. The first term in the current noise expression depends on the gate current (typically less than 1×10^{-15} A for CMOS transistors) and the second term is proportional to frequency squared. As a result, generally the current noise of a CMOS OTA is only significant at frequencies that are well above the maximum

frequency of interest for a VLF receiver. The voltage noise from the OTA depends on the transconductance of the input differential pair. The voltage noise can be reduced by increasing g_{m1}, which corresponds to increasing the bias current. The OTA noise expressions shown above include thermal noise and shot noise. A detailed analysis of the OTA noise performance is given in Section 4.3.2, which also includes the effect of $1/f$ noise.

The distortion of the gain stage is important because it processes large signals with considerable gain. In particular, the amplifier that drives the final output will limit the distortion performance because it handles the largest signal swings. The linearity is maximized through the use of feedback. A basic negative feedback block diagram is shown in Figure 4.5. The circuit consists of a forward amplifier with gain a and a feedback network with gain f. In the LNA gain stage, the forward amplifier is an OTA and the feedback network is a resistive network. The gain of the basic feedback network is

$$\frac{v_{\mathrm{o}}}{v_{\mathrm{i}}} = \frac{a}{1+af} \tag{4.21}$$

The loop gain is defined as $T = af$. If the loop gain is much greater than one then the gain of the feedback circuit simplifies to

$$\frac{v_{\mathrm{o}}}{v_{\mathrm{i}}} = \frac{1}{f} \tag{4.22}$$

Feedback has a number of benefits, including the fact that the gain of the system depends only on the feedback factor f if the loop gain is large. Feedback also has an effect on the distortion performance of the system [40]. The harmonic distortion can be represented in terms of the HD_2 and HD_3, which are the ratio of the amplitude of the 2nd and 3rd harmonic to the amplitude of the fundamental. When feedback is applied the HD_2 and HD_3 become

$$HD_{2,\mathrm{FB}} = \frac{1}{(1+a_1 f)^2} HD_2 \tag{4.23}$$

$$HD_{3,\mathrm{FB}} = \frac{\left|1 - \frac{2a_2^2 f}{a_3(1+a_1 f)}\right|}{(1+a_1 f)^3} HD_3 \tag{4.24}$$

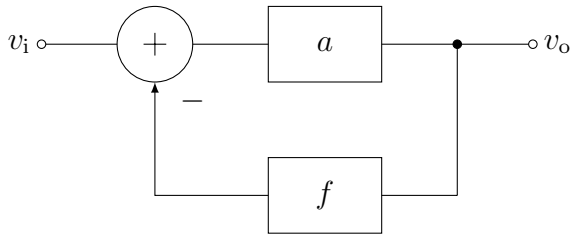


Figure 4.5: Block diagram of the ideal feedback configuration.

Applying feedback improves the HD_2 by a factor of $(1+T)^2$ and the HD_3 by a factor of $(1+T)^3$. Clearly, increasing the loop gain can lead to significant increases in the linearity of the amplifier.

Several strategies have been applied to ensure the best possible linearity of the gain stage. First, the OTAs were designed to have a large DC gain and maximum possible signal swing. Given the low frequency of the receiver, the bandwidth of the amplifiers is not a significant concern so the OTAs are optimized for high DC gain. Second, the gain in the gain stage is split into two parts, which results in a larger feedback factor for each section and therefore a larger loop gain for each section. Third, it is expected that the switches used to select the R_4 resistor will introduce some nonlinearity. As a result, the switchable resistor is placed in the first section of the gain stage where the signal swings are smaller and the switch nonlinearity will have a smaller effect. Fourth, since the output amplifier will contribute most significantly to the distortion performance, a relatively small gain of three is implemented with R_1 and R_2 to ensure that the loop gain is as large as possible in this section of the gain stage.

4.1.4 Auto-Bias Circuit

Due to the unique nature of the circuits used in the LNA, biasing can be a challenge. In the gain stage a constant-g_m current source is used to give consistent performance over variations in process, voltage and temperature. However, the input stage of the LNA is more difficult to properly bias due to the fact that its output DC voltage depends on the NPN collector current and on the load resistor value, both of which

can vary significantly. The output DC voltage is given by

$$V_{\mathrm{OUT}} = V_{\mathrm{DD}} - I_{\mathrm{C}} R_{\mathrm{L}} \tag{4.25}$$

If the DC output voltage varies too much, it may go out of the suitable input range of the gain stage causing the receiver to not function properly. In past designs, this problem has been overcome by setting the NPN bias voltage externally using a potentiometer. Using this method the voltage can be tuned to produce the proper bias point. However, this approach has a serious drawback. While the bias point can be properly tuned when the receiver is initially deployed, the bias point may shift over time due to changes in temperature or component drift. Recall that the collector current of the NPN is

$$I_{\mathrm{C}} = I_{\mathrm{S}} \exp\left(\frac{V_{\mathrm{bias}}}{kT/q}\right) \tag{4.26}$$

which depends directly on temperature [25].

To overcome this problem an automatic biasing system has been implemented. The auto-bias circuit is shown in Figure 4.6. The circuit operates by measuring the DC voltage at the output of the input stage using a common-mode detector. The common-mode detector consists of two large resistors that calculate the average of the differential outputs, which is effectively the DC output voltage. The DC output voltage is then compared with the desired output voltage, V_{ref}. The difference between the actual DC output voltage and the desired voltage is amplified with an error amplifier and fed back to the input stage transistors. Essentially, this negative feedback loop automatically adjusts the bias voltage to ensure that the output DC voltage is equal to the reference voltage. In this design, the reference voltage is set to $V_{\mathrm{DD}}/2$ in order to keep the outputs centered between the two supply rails. This auto-bias strategy is similar to how a common-mode feedback circuit controls the DC output voltage of a fully-differential OPAMP.

There are two important considerations for the design of the auto-bias circuit. First, the resistors in the common-mode detector must be very large to ensure that they don't reduce the output impedance of the input stage and so that they don't adversely affect the noise performance of the input stage. To satisfy this requirement

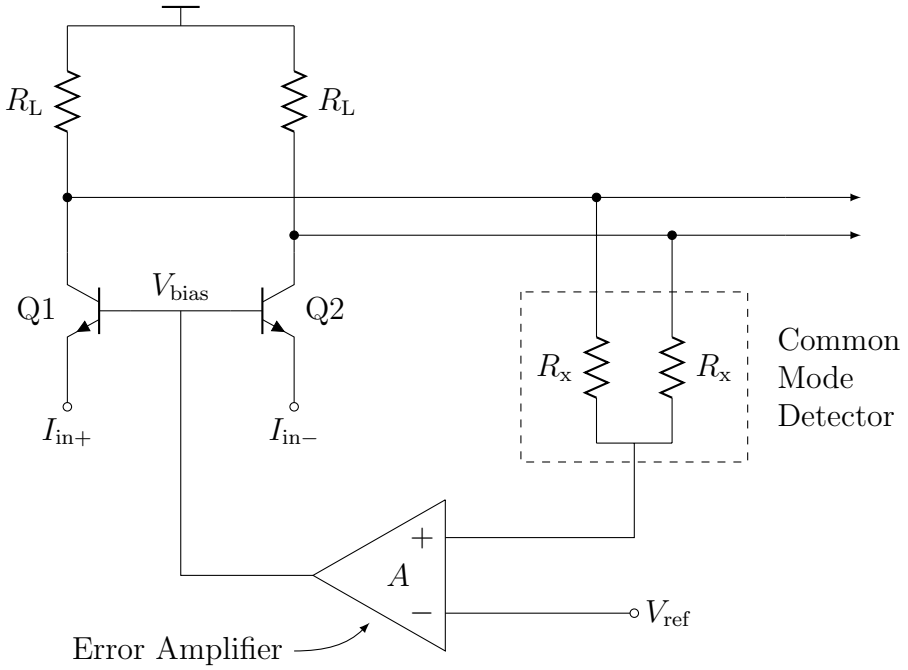


Figure 4.6: Schematic of the auto-bias circuit and its connection to the input stage.

the resistors are each 1 MΩ. Second, the error amplifier itself must be robust to changes in temperature and component drift, otherwise the auto-bias circuit will fail to operate properly. This is accomplished by using a constant-g_{m} current source to bias the error amplifier.

The architecture for the error amplifier is shown in Figure 4.7. It is a single-stage differential pair amplifier with a current mirror load. The single-stage architecture provides the benefit of easing the requirements for stabilizing the feedback loop because it only produces a single dominant pole, while still giving more than enough DC gain for the feedback loop to operate correctly.

Transistor-level simulations were performed to validate the auto-bias circuit. Figure 4.8 shows the LNA transimpedance gain as a function of the temperature of the LNA over a range of −80° C to 120° C. This simulation includes transistor-level circuits for the input stage, gain stage, auto-bias circuit and all other relevant circuit blocks. The red curve represents the performance when the LNA is biased using a manual bias voltage that is set external to the chip. In this case, the manual bias

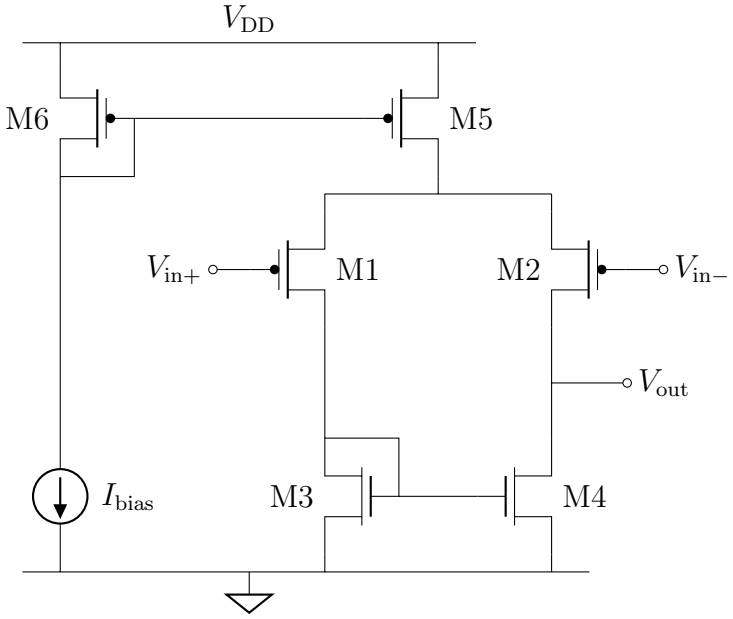


Figure 4.7: Schematic of the error amplifier used in the auto-bias circuit.

voltage was set for optimal performance at around 25° C. Notice how the gain is consistent over a limited range of roughly ±10° C. Outside of this range the gain of the amplifier falls dramatically, which indicates that the LNA is no longer operating properly. Temperature variations of this amount could easily be encountered between day and night and between different seasons when the receiver is deployed. The blue curve represents the performance when the auto-bias circuit is enabled. With the auto-bias circuit the gain is consistent over the entire range of temperatures, with a variation of less than 1 dB.

4.2 ADC Implementation

The ADC was implemented with a fully-differential continuous-time delta-sigma modulator. The primary reason this ADC architecture was selected was that it has an implicit anti-alias filter. In previous VLF receiver designs the AAF has used a large percentage of the total power consumption of the signal path blocks (LNA, AAF and ADC). For example, in the Penguin receiver the AAF used 47% of the total

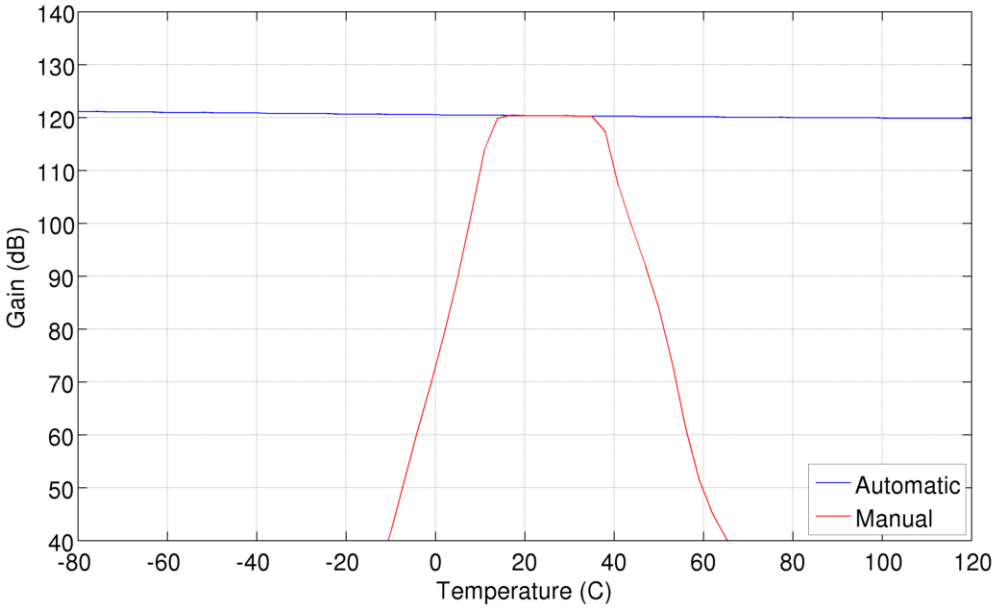


Figure 4.8: LNA temperature sweep simulation.

signal path power [32]. Eliminating the AAF can result in significant power savings. Additionally, delta-sigma modulators are robust to mismatch in their components. Mismatch is often a key contributor to distortion in differential circuits. In fact, past ADC designs for VLF receivers have required calibration to achieve over 90 dB SFDR [49]. Delta-sigma modulators provide a notable advantage in terms of their insensitivity to mismatch when compared with other ADC architectures. Together, these qualities make the continuous-time delta-sigma modulator an ideal candidate for the single-chip VLF receiver.

4.2.1 Loop Filter Design

A third-order modulator with a single-bit quantizer was used in this design. The third-order loop filter provides good quantization noise suppression at a reasonable oversampling ratio without running into the stability problems seen with higher order loop filters. The oversampling ratio is set to 150, which at a 100 kHz Nyquist sampling rate results in an ADC clock frequency of 15 MHz. The single-bit quantizer was

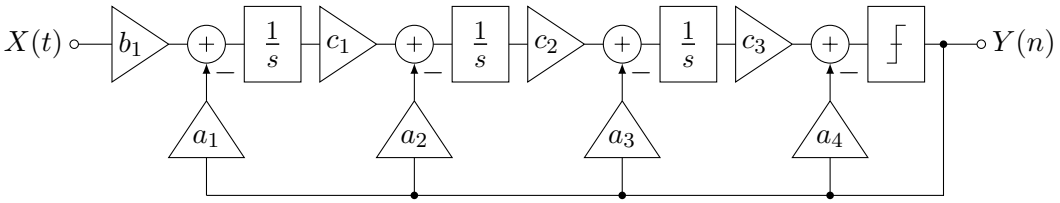


Figure 4.9: Block diagram of the third-order continuous-time delta-sigma modulator.

selected for its perfect linearity, which is due to it only having two levels. Using a multi-bit architecture would have added unnecessary complexity and made achieving the stringent linearity goal even more challenging.

The modulator block diagram is shown in Figure 4.9. A distributed feedback architecture was used, which is evident because of the multiple feedback paths that connect to the loop filter. The distributed feedback architecture was selected for its superior anti-alias filtering characteristic. The third-order loop filter consists of three continuous-time integrators that are represented by the $1/s$ blocks. The modulator has several gain coefficients. The input signal is scaled with an input coefficient, b_1. The output of each integrator is scaled with its own scaling coefficient, c_n. Similarly, each feedback path has its own gain coefficient, a_n. Finally, a single-bit comparator with a half-sample delay was used for the quantizer in this design. Although a typical third-order distributed feedback modulator would only have three feedback coefficients, this design includes a fourth feedback coefficient, a_4, which is used to compensate for the effect of the half-sample delay.

The loop filter design begins with the design of a discrete-time loop filter, which was later converted to a continuous-time filter. The discrete-time loop filter was designed using the Delta Sigma Toolbox [44]. This toolbox includes dozens of functions for the design, synthesis and simulation of delta-sigma modulators in the MATLAB environment. Here it was used to generate optimal gain coefficients for the discrete-time loop filter given the filter order, oversampling ratio, out-of-band gain and filter type. Figure 4.10 shows the resulting discrete-time loop filter noise transfer function and signal transfer function. The horizontal axis in this plot is frequency and the vertical axis is the response in dB. The blue curve shows the NTF. At low frequencies the NTF rolls off at a rate of 60 dB/decade, which is consistent with a third-order

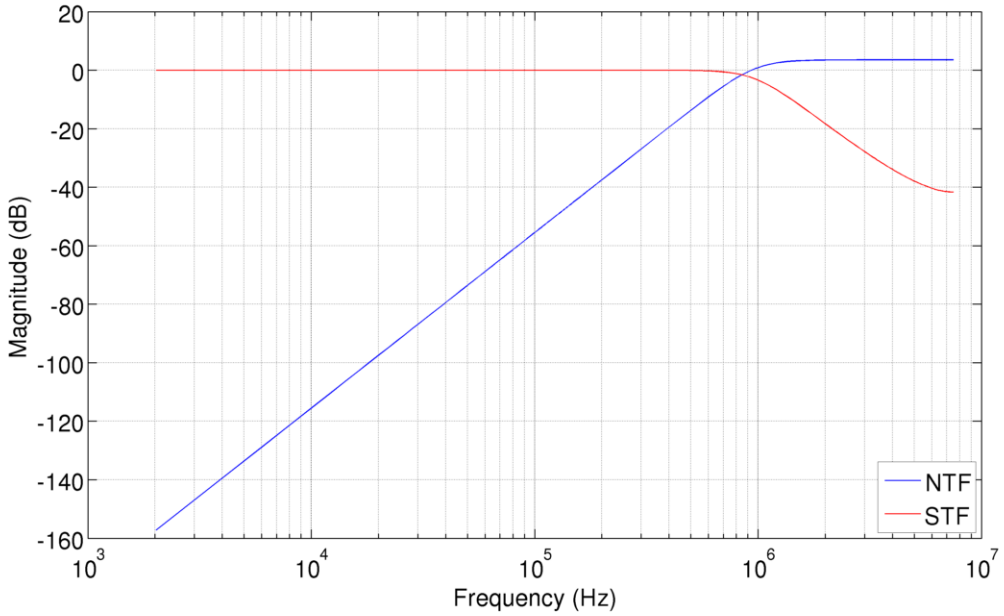


Figure 4.10: Noise transfer function and signal transfer function of the modulator.

filter. At high frequencies the maximum gain of the NTF is set to 1.5 in order to satisfy the modified Lee criterion for single-bit modulator stability [45, 10]. The STF is flat over the signal band, as expected.

A common modification to the standard loop filter is to optimize the placement of the NTF zeros [45]. Spreading the zeros throughout the signal band can further reduce the in-band quantization noise and therefore increase the SQNR at the same oversampling ratio. For example, a third-order loop filter with optimized zeros gives an SQNR improvement of 8 dB. Zero optimization is accomplished in a third-order loop filter by adding an additional feedback path from the output of the third integrator to the input of the second integrator. This additional feedback path is generally implemented with a resistor. Unfortunately, in this design the additional feedback path would require a resistor with a value of over 50 MΩ, which was not practical to implement in an integrated circuit. For this reason, non-optimized zeros are used in this design.

The discrete-time loop filter was converted to a continuous-time loop filter using the impulse-invariant transform [13]. This method determines the continuous-time

loop filter coefficients that result in an equivalent impulse response when measured at the sampling instants. This is done by setting the impulse response of the discrete-time loop filter equal to the impulse response of the continuous-time loop filter. This relationship can be expressed as

$$\mathcal{Z}^{-1}\left\{H(z)\right\} = \mathcal{L}^{-1}\left\{R_{\mathrm{DAC}}(s)H(s)\right\}|_{t=nT_s} \tag{4.27}$$

where $\mathcal{Z}^{-1}$ is the inverse z-transform, $\mathcal{L}^{-1}$ is the inverse Laplace transform and $R_{\mathrm{DAC}}(s)$ is the DAC transfer function used in the continuous-time modulator implementation.

After conversion, the outputs of the integrators are scaled to limit their signal swing. This process is referred to as dynamic range scaling and is accomplished by adjusting the c_n coefficients in the loop filter. It is important to note that changes to the c_n coefficients will also require changes to the other coefficients in order to maintain the same loop filter response. With a continuous-time modulator, behavioral simulations are needed to determine the scaling coefficients because the discrete-time model in MATLAB only predicts the integrator outputs at the sampling instants. The integrator outputs in a continuous-time modulator may have larger values between samples.

The signal swing at the output of the integrators is directly linked to the distortion performance of the ADC. Small signal swings will result in better distortion performance because the OTAs have less non-linearity with smaller signal swings. Unfortunately, the scaling also affects the size of the capacitors in the integrators. More scaling results in larger capacitances, which will negatively affect the frequency response of the OTAs. Therefore, a design trade-off exists where the amount of scaling has be chosen to give the desired distortion performance while not impacting the OTA performance. The most important integrator for distortion performance is the first stage, because any errors in the first stage are referred directly to the input. Distortion caused by the later integrator stages will have a smaller effect because the error occurs at less sensitive points in the modulator. For this reason, the first integrator is scaled to have a maximum signal swing of 40% full scale, while the second

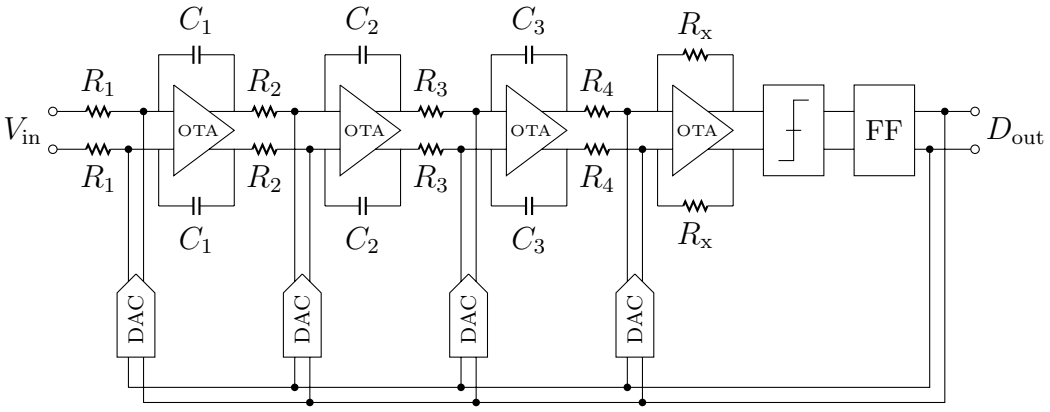


Figure 4.11: Schematic of the third-order continuous-time delta-sigma modulator.

and third integrators are scaled to have a swing of 50% full scale.

4.2.2 Modulator Architecture

The top-level schematic of the continuous-time delta-sigma modulator is shown in Figure 4.11. The modulator consists of three continuous-time integrator stages, followed by a summation amplifier, a comparator, a flip-flop and four feedback DACs. The input signal is a differential voltage with a full scale range that extends from ground to the supply rail (1.2 V). The output of the modulator is a 1-bit digital signal. Both the non-inverted and inverted output signal are used by the modulator, but only the non-inverted signal is buffered and sent off-chip.

The filter stages are implemented with active-RC integrators. There are many different continuous-time integrator architectures, but the active-RC circuit was selected because it offers the highest linearity. The transfer function of the active-RC integrator is

$$H(s) = \frac{1}{sRC} \tag{4.28}$$

where R is the input resistor and C is the integrating capacitor [38]. This relationship can be used to calculate the resistor and capacitor values that implement the correct loop filter gain coefficients. In many cases, the value of the resistor is set by the noise requirement, and the gain coefficient is used to determine the appropriate capacitor

value.

A dynamic comparator is used to implement the single-bit quantizer in this modulator. A flip-flop follows the comparator to capture its output value and add a half-sample delay. The half-sample delay serves two purposes. First, it gives the comparator a half-sample to settle to its final value before the value is captured by the flip-flop. This reduces the speed requirement on the comparator. Second, it eliminates the effect of signal-dependent delay. A common problem with dynamic comparators is that the settling time of the output depends on the input value. This causes errors in the modulator feedback path and adversely affects the noise shaping performance. By adding a fixed half-sample delay before the flip-flop captures the comparator output, the signal-dependent delay problem of the quantizer is eliminated.

Unfortunately, adding a half-sample delay to the modulator changes the transfer function and itself reduces the noise shaping performance. This negative effect can be exactly canceled by adding an additional feedback path at the input of the comparator, which is implemented with the fourth DAC (a_4 coefficient). The value of a_4 is selected to match the impulse response of the half-sample delayed loop filter to the ideal discrete-time loop filter that the design is based upon [3].

The overall performance of the modulator is largely determined by the noise performance. There are two sources of noise in the modulator: quantization noise and circuit noise. The quantization noise is caused by the error introduced in the quantizer. This noise is shaped by the delta-sigma modulator. As a result, the amount of quantization noise in the signal band is determined by the loop filter design, which was discussed in the previous section. The circuit noise is caused by thermal noise, flicker noise and other noise sources in the passive and active components that are used to implement the modulator. Typically the quantization noise is designed to be 10 dB to 20 dB below the circuit noise in order to allocate as much of the noise budget as possible to the circuit noise. This design strategy has the added benefit of allowing extra margin for the quantization noise shaping to be degraded by mismatch or other non-ideal effects in the circuit without adversely affecting the overall performance of the ADC.

The total allowable input referred noise power as a function of the resolution of

the ADC is given by

$$\overline{v_{\mathrm{n}}^2} = \frac{V_{\mathrm{FS}}^2}{12\left(2^B - 1\right)^2} \tag{4.29}$$

where V_{FS} is the full-scale voltage of the ADC, and B is the desired resolution. In this design the quantization noise is set to be about 20 dB below the circuit noise. Therefore, the contribution of quantization noise is negligible and the majority of the noise power can be allocated to circuit noise.

The modulator circuit noise performance is limited by the circuit components connected to the input of the modulator. Later stages of the modulator don't contribute significant noise because of the gain that precedes them. Figure 4.12 shows a simplified schematic of the first stage of the modulator for noise analysis. The circuit includes the first active-RC integrator stage and the resistor from the first feedback DAC. There are three noise sources: the input resistor R, the DAC resistor R_{DAC} and the OTA. The values of the noise sources are

$$\overline{v_{\mathrm{R}}^2} = 4kTR\Delta f \tag{4.30}$$

$$\overline{v_{\mathrm{DAC}}^2} = 4kTR_{\mathrm{DAC}}\Delta f \tag{4.31}$$

$$\overline{v_{\mathrm{OTA}}^2} = 4kT\frac{\gamma_{\mathrm{p}}}{g_{\mathrm{m1}}}\left(1 + \frac{\gamma_{\mathrm{n}}}{\gamma_{\mathrm{p}}}\frac{g_{\mathrm{m3}}}{g_{\mathrm{m1}}}\right)\Delta f + \left(\frac{K_{\mathrm{fp}}}{C_{\mathrm{ox}}}\frac{1}{W_1L_1} + \frac{K_{\mathrm{fn}}}{C_{\mathrm{ox}}}\frac{1}{W_3L_3}\frac{g_{\mathrm{m3}}^2}{g_{\mathrm{m1}}^2}\right)\frac{\Delta f}{f} \tag{4.32}$$

The resistors contribute thermal noise, while the OTA contributes both thermal and $1/f$ noise. A detail analysis of the OTA noise performance is given in Section 4.3.2. All of these noise sources can be referred to the input of the ADC to determine the total input referred noise. The value of each noise source when referred to the input is given by

$$\overline{v_{\mathrm{i,R}}^2} = \overline{v_{\mathrm{R}}^2} \tag{4.33}$$

$$\overline{v_{\mathrm{i,DAC}}^2} = \overline{v_{\mathrm{DAC}}^2}\left(\frac{R}{R_{\mathrm{DAC}}}\right)^2 \tag{4.34}$$

$$\overline{v_{\mathrm{i,OTA}}^2} = \overline{v_{\mathrm{OTA}}^2}\left(1 + \frac{R}{R_{\mathrm{DAC}}}\right)^2 \tag{4.35}$$

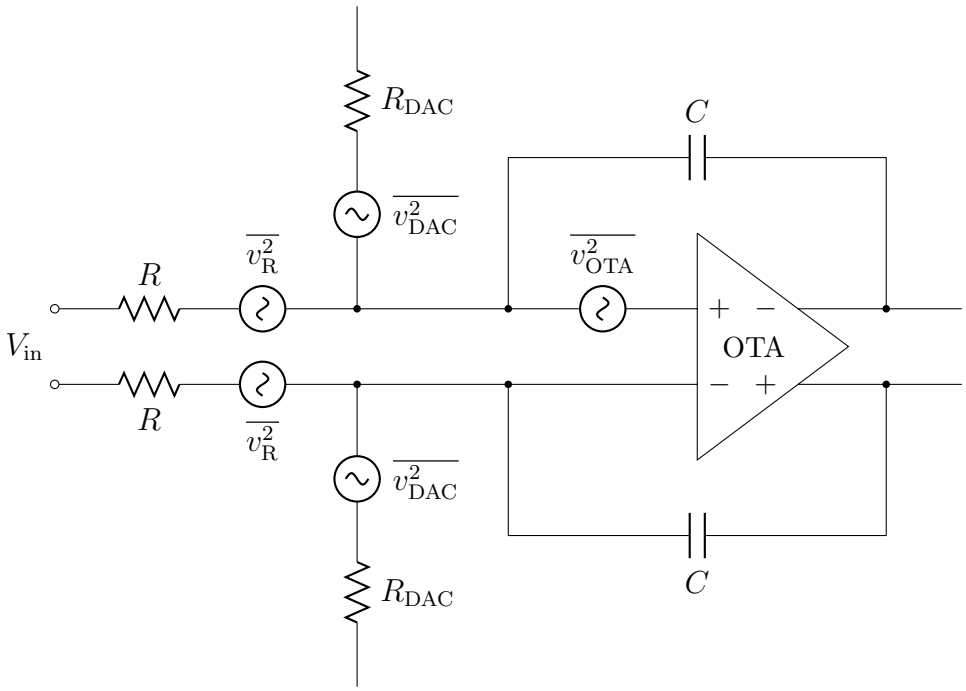


Figure 4.12: Simplified schematic of the first stage of the modulator for noise analysis.

The noise from the input resistor is unchanged, but the other noise sources are modified when referred to the input. The total input referred noise of the delta-sigma modulator can be calculated by summing these values, which gives

$$\overline{v_{\mathrm{i}}^2} = 2\left(\overline{v_{\mathrm{R}}^2} + \overline{v_{\mathrm{DAC}}^2}\left(\frac{R}{R_{\mathrm{DAC}}}\right)^2 + \overline{v_{\mathrm{OTA}}^2}\left(1 + \frac{R}{R_{\mathrm{DAC}}}\right)^2\right) \tag{4.36}$$

where the factor of two is due to the fact that the modulator is a differential circuit. In this design, the loop filter input coefficient b_1 is equal to the first feedback coefficient a_1, which results in $R = R_{\mathrm{DAC}}$. This relationship can be used to simplify the total input referred noise expression above.

There are two competing goals when designing the first stage of the modulator. The first goal is meeting the noise requirement, which mandates that small resistance values be used to stay within the noise budget set by Equation 4.29. The second goal is minimizing the distortion, which requires that large resistance values be used because they lead to better linearity from the modulator [5]. To satisfy both requirements, the

resistance values are set to the maximum value that still meets the noise requirement. Further, since it is desirable to make the resistors as large as possible, the majority of the noise in the first stage is allocated to the resistors. In this design 80% of the noise budget is allocated to the resistors and 20% is allocated to the OTA. Reducing the noise contribution from the OTA requires increasing the power dissipation. The slightly higher power dissipation will have to be tolerated in order to achieve the stringent linearity goals.

The later integrator stages are not as critical to the overall noise and distortion performance of the modulator, which means that the design constraints on the passive components and on the OTA in these stages are relaxed. The noise requirements are not as high for the later stages because of the gain of the stages that precede them. The distortion requirement is also not as aggressive because errors introduced by the later stages are rejected by the noise shaping effect of the modulator. These reduced requirements lead to larger resistors, smaller integrating capacitors and lower-power OTAs. As a result, the power dissipation of the ADC can be optimized by scaling back the power dissipation of the later integrator stages.

There are four OTAs in the modulator, each with a different design objective. The most stringent requirements are in the design of the input stage OTA, which requires very low noise, high gain and minimal distortion. The requirements are reduced for the OTAs in the second and third integrators. The OTA used in the summation amplifier is designed for maximum bandwidth with lower gain. A two-stage Miller compensated OTA architecture is used to implement all of the OTAs. The same architecture is also used to implement the OTAs in the LNA portion of the receiver. The design of the two-stage Miller compensated OTA is discussed separately in Section 4.3.

4.2.3 Circuit Blocks

The modulator uses a single-bit quantizer that is implemented with a regenerative latch comparator [4]. Figure 4.13 shows the schematic of the comparator circuit. The circuit consists of two cross coupled transistor pairs, one PMOS and one NMOS,

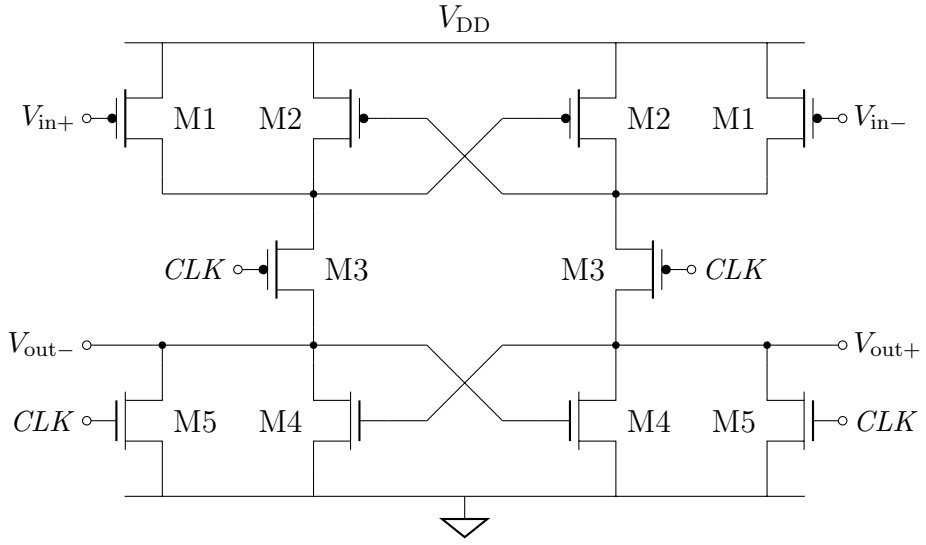


Figure 4.13: Schematic of the regenerative latch comparator.

which create a positive feedback loop. It also has a differential input and differential output, as well as a clock signal which controls the latch. The comparator is a dynamic circuit, which means that it ideally has no DC power consumption.

The basic operation of the comparator has two phases. In the first clock phase, when the clock is high, the comparator is reset by the two M5 transistors that pull the outputs to ground. The positive feedback loop is disconnected in the reset mode by disabling the two M3 transistors. The second phase occurs when the clock is low. As soon as the clock goes low the regenerative latch is enabled and the comparator makes a decision based on the difference between the two inputs. This decision is latched and doesn't change until the comparator is reset again.

The comparator is the least critical block in the continuous-time delta-sigma modulator because any error introduced by the comparator is rejected by the full noise shaping effect of the modulator. As a result, the offset and hysteresis of the comparator are not critical design constraints. Instead, the primary design constraint for the comparator is the timing constraint. Namely, the output of the comparator must settle to its final value within a half sample. After a half sample the value is captured by the flipflop. The regenerative latch settling time is only a small fraction of the half sample requirement, so the transistors are sized to reduce power consumption while

still comfortably meeting the timing constraint.

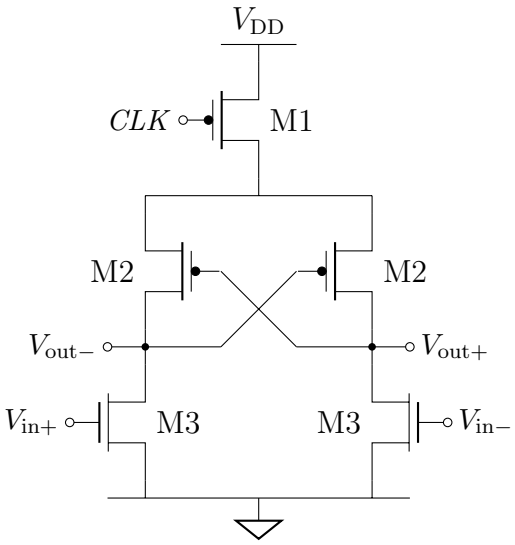
The flipflop is implemented with a differential semistatic flipflop [52]. The flipflop uses a standard master-slave architecture, which consists of two latches where the output of the master latch is connected to the input of the slave latch. The master latch is shown in Figure 4.14a. It is a dynamic latch that has high speed and low power consumption. It consists of a cross-coupled PMOS pair and has a differential input and output. The slave latch is shown in Figure 4.14b. The slave latch is a static latch, which ensures that the outputs of the flipflop are firmly set to the positive and negative rails. A differential flipflop is used because the feedback DACs each require the non-inverted and inverted output values. By using a differential flipflop it is not necessary to use an inverter to generate the complementary signal, which could lead to problems with unequal delay.

Both the master latch and the slave latch run on the same clock phase, which is referred to as single-phase clocking. The comparator is also designed to run with the same clock phase. Therefore, all of the clocked circuits in the ADC run on the same clock phase. This greatly simplifies the clock generation and distribution network on the test chip as there is no need to generate and synchronize an inverted clock signal.

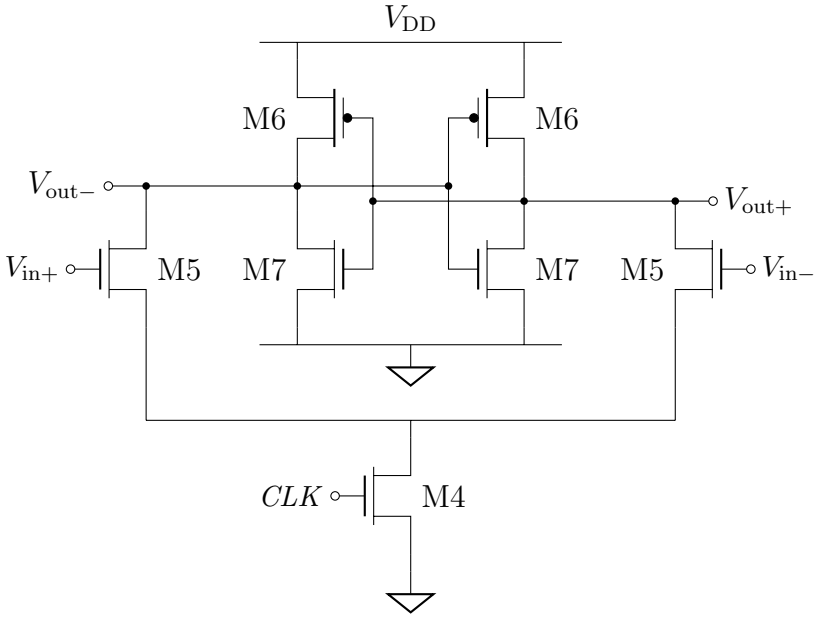
The feedback DACs are implemented with a current-steering DAC that uses a resistance to set the value of the feedback current. Figure 4.15 shows the schematic of the DAC. The DAC is a differential circuit and consists of two resistors, with value R_{DAC}, that are connected to either the positive reference voltage or the negative reference voltage depending on the value of the modulator output. The inputs to the DAC are a complementary digital signal, which means that one of the resistors is connected to the positive reference while the other is connected to the negative reference. In this design the reference voltages are set to ground and V_{DD}, so the value of each DAC resistance can be calculated with

$$R_{\mathrm{DAC}} = \frac{V_{\mathrm{DD}}}{a_n f_{\mathrm{s}} C_n} \tag{4.37}$$

where a_n is the loop filter feedback coefficient, f_{s} is the sampling rate and C_n is the value of the integrating capacitor.



(a) Master latch.



(b) Slave latch.

Figure 4.14: Schematic of the semistatic flipflop.

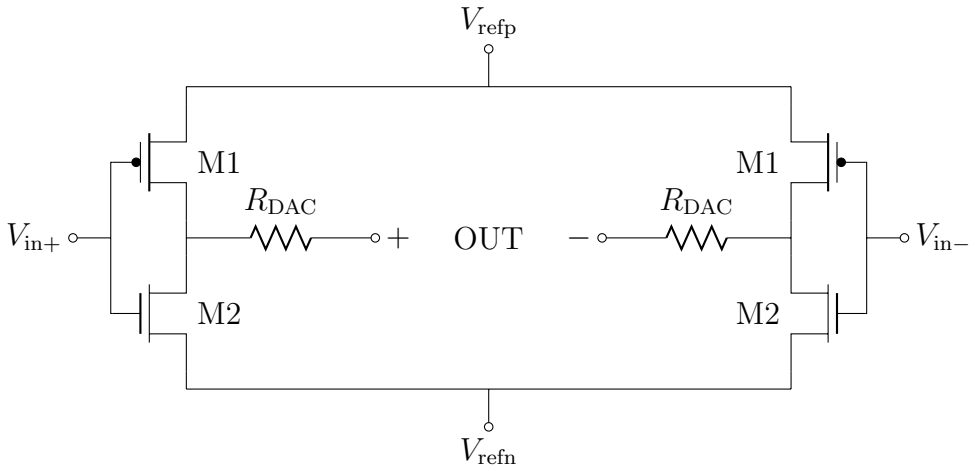


Figure 4.15: Schematic of the current-steering feedback DAC.

The single-bit DAC is inherently linear, so the primary concern in the DAC design is matching the positive and negative slope of the feedback current to prevent inter-symbol interference. This is accomplished by properly setting the ratio of the width of the PMOS to NMOS transistors in the DAC. In this design, the PMOS transistors are three times wider than the NMOS transistors.

In a discrete-time delta-sigma modulator the loop filter gain coefficients are implemented with ratios of capacitors, which are typically accurate to within 1% if proper layout techniques are applied [29]. On the other hand, in a continuous-time delta-sigma modulator the gain coefficients are set by the RC products in the active-RC integrators. Process variations of 10% to 20% are not uncommon for integrated resistors and capacitors, which can result in an RC product variation of over 30% [38]. This RC product variation changes the loop filter coefficients and can lead to reduced noise shaping, and in severe cases it can cause modulator instability.

To overcome this problem the integrating capacitors (C_1-C_3) are tunable. This allows for the values of the capacitors to be changed to compensate for the process variations of the RC products. Figure 4.16 shows the schematic of the tunable capacitor [50]. The circuit uses a single fixed capacitor plus three binary weighted unit capacitors. The three control bits give a total of eight capacitance values. The switches are implemented with CMOS transmission gates. The total capacitance of

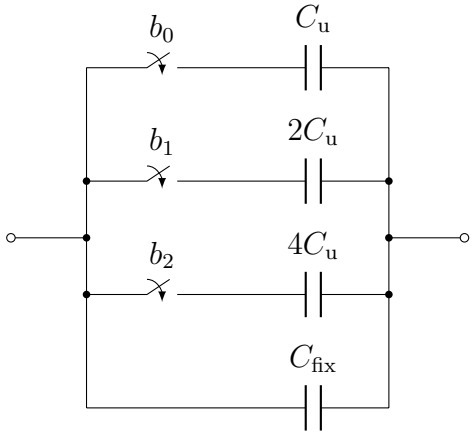


Figure 4.16: Schematic of the tunable capacitor.

the bank is given by

$$C_\mathrm{bank} = C_\mathrm{fix} + C_\mathrm{u} \sum_{i=0}^{2} b_i 2^i \tag{4.38}$$

where $[b_2 b_1 b_0]$ is the 3-bit control signal. The fixed capacitance, C_fix, and the unit capacitance, C_u, are selected to implement the desired capacitance value with a tuning range of -30% to $+40\%$ with 10% steps. In this application, the capacitors are tuned manually using external control signals. The appropriate tuning value can be determined by trial and error or by measuring the provided on-chip test structures.

4.3 OTA Implementation

Operational transconductance amplifiers (OTAs) are used throughout the receiver design. The LNA uses three OTAs: two single-ended OTAs at the input of the gain stage and one fully-differential OTA at the output of the gain stage. The ADC uses four OTAs: three fully-differential OTAs in the RC integrator stages and one fully-differential OTA in the summation amplifier.

This section covers the design of the OTA circuit that is employed throughout the receiver. A common architecture has been selected for simplicity, which is then optimized to fit the requirements of each individual amplifier. For example, the OTA in the first RC integrator stage in the ADC requires a low-noise OTA with high gain,

Table 4.1: OTA architecture performance comparison.

Architecture	Gain	Output Swing	Speed	Power	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-Cascode	Medium	Medium	High	Medium	Medium
Two-Stage	High	Highest	Low	Medium	Low
Gain-Boosted	High	Medium	Medium	High	Medium

while the ADC summation amplifier OTA requires high-bandwidth and low-power. These are very different design goals, but both of these OTAs are successfully implemented with the same OTA architecture using different design parameters (transistors sizes and bias currents).

It is important to point out the distinction between OTAs and OPAMPs. The difference between an OTA and an OPAMP lies in its output stage. An OTA has a large output impedance, which generally makes it only useful for driving high impedance loads. On the other hand, an OPAMP includes an output buffer that has a low output impedance and is capable of driving low impedance loads. While the circuit presented in this section may be commonly referred to as an OPAMP, technically it is an OTA due to its high output impedance.

4.3.1 Architecture Comparison

There are a number of different amplifier architectures that could be used in the receiver, each with its own advantages and disadvantages. Table 4.1 shows a comparison of four popular OTA architectures in terms of their gain, output swing, speed, power dissipation and noise [42]. The four architectures are the telescopic OTA, the folded-cascode OTA, the two-stage OTA and the gain-boosted OTA.

There are four main requirements for the OTA used in this design. First, it must have a large DC gain to ensure good linearity of the system. Recall that the harmonic distortion is directly related to the loop gain, which itself depends on the DC gain of the amplifiers. Second, the OTA noise must be low to give good overall receiver sensitivity without consuming unnecessary power. Third, the amplifier must have a

large available output swing to accommodate large signal swings without degrading the performance. Finally, the receiver runs on a 1.2 V supply voltage, which limits the available headroom. As a result, the amplifier must have a minimum number of vertically stacked transistors.

The two-stage OTA architecture most closely fits the requirements outlined above and is selected for use in this design. This architecture has high gain, the highest output swing, and low noise. The one downside of the two-stage architecture is its speed, but the bandwidth of the VLF receiver is low so speed is not a critical requirement.

4.3.2 Two-Stage OTA

This section covers the design and analysis of the fully-differential version of the two-stage Miller compensated OTA architecture [25]. A single-ended version of the circuit is also used in the receiver and many of the results for the fully-differential version also apply to the single-ended version. The schematic of the fully-differential version of the two-stage OTA architecture is shown in Figure 4.17. The circuit uses only CMOS transistors and consists of two amplification stages.

The gain of the two-stage OTA can be calculated by considering the two stages separately. The first stage consists of the input transistor, M1, and the current source loads, M3. The gain of the first stage is

$$A_{\mathrm{v1}} = g_{\mathrm{m1}} \left(r_{\mathrm{o1}} \parallel r_{\mathrm{o3}} \right) \tag{4.39}$$

where g_{m1} is the transconductance of M1, r_{o1} is the output impedance of M1 and r_{o3} is the output impedance of M3. The second stage, which consists of transistor M2 and current source load M4, has a gain of

$$A_{\mathrm{v2}} = g_{\mathrm{m2}} \left(r_{\mathrm{o2}} \parallel r_{\mathrm{o4}} \right) \tag{4.40}$$

where g_{m2} is the transconductance of M2, r_{o2} is the output impedance of M2 and r_{o4} is the output impedance of M4. The total gain of the OTA can be calculated by

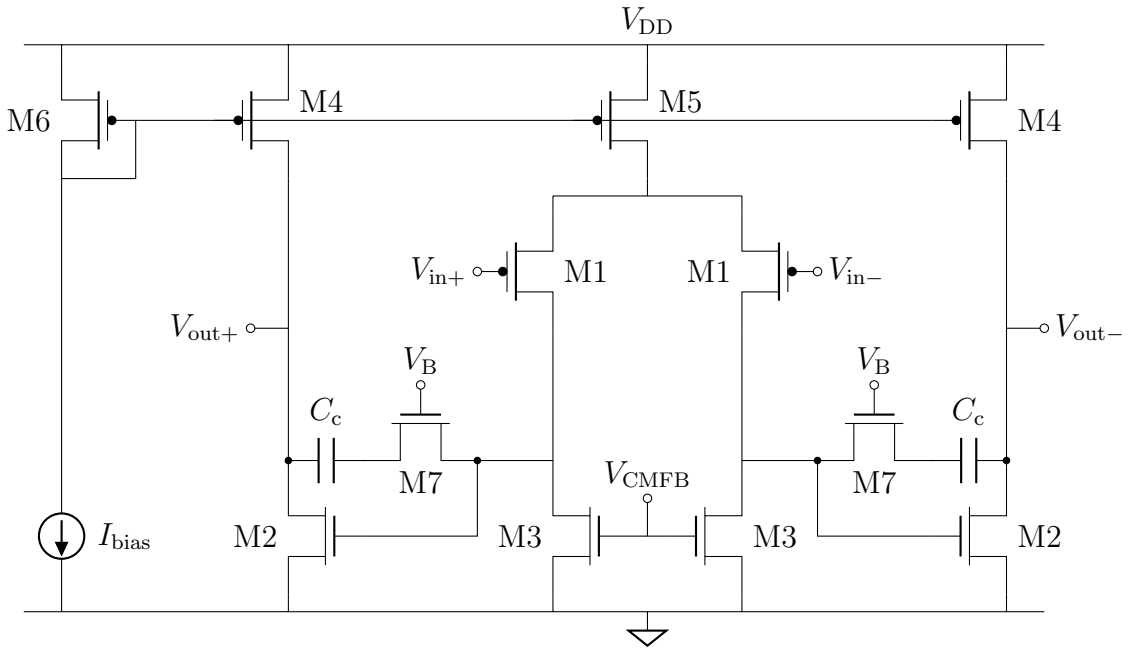


Figure 4.17: Schematic of the fully-differential two-stage OTA.

combining the gain from the first stage and the gain from the second stage, which gives a total gain of

$$A_v = A_{v1}A_{v2} = g_{m1}\left(r_{o1} \parallel r_{o3}\right) g_{m2}\left(r_{o2} \parallel r_{o4}\right) \tag{4.41}$$

The gain of the amplifier can be increased by increasing the channel length of the transistors, which results in a larger output impedance and therefore higher gain.

The input impedance of the amplifier is essentially infinite due to the PMOS differential pair at the input. The PMOS transistors present a capacitive load to the driving circuit. The output impedance of the amplifier depends on the output stage transistors and is

$$R_{out} = r_{o2} \parallel r_{o4} \tag{4.42}$$

The large output impedance gives a large gain for the output stage, but limits the types of loads that the amplifier can drive. For example, a small resistive load will reduce the gain of the amplifier because it is in parallel with the output impedance.

One of the key advantages of the two-stage OTA architecture is the output range. Because there are no cascoded transistors in the output stage, the output voltage can swing within one overdrive voltage of the supply rails. Therefore, the output range is

$$V_{\mathrm{ov2}} <= V_{\mathrm{o}} <= V_{\mathrm{DD}} - V_{\mathrm{ov4}} \tag{4.43}$$

where V_{ov2} is the overdrive voltage of M2 and V_{ov4} is the overdrive voltage of M4. The output range can be maximized by reducing these overdrive voltages by increasing the W/L (width over length) ratios of the output transistors.

The input offset voltage of a fully-differential amplifier is defined as the differential input voltage that results in zero differential output voltage. The offset can be calculated as a function of the mismatch between pairs of components in the amplifier circuit. The input offset voltage of the two-stage OTA is

$$V_{\mathrm{offset}} = \Delta V_{\mathrm{t1}} + \Delta V_{\mathrm{t3}} \left(\frac{g_{\mathrm{m3}}}{g_{\mathrm{m1}}} \right) + \frac{\Delta V_{\mathrm{ov1}}}{2} \left(\frac{\Delta (W/L)_3}{(W/L)_3} - \frac{\Delta (W/L)_1}{(W/L)_1} \right) \tag{4.44}$$

where ΔV_{t1} is the difference between the threshold voltage of the two M1 transistors, $\Delta (W/L)_3$ is the difference between the width over length ratio of the two M3 transistors, and so forth. The offset voltage can be reduced by using a longer channel length for M3 than M1, which gives a small $g_{\mathrm{m3}}/g_{\mathrm{m1}}$ ratio. It can also be reduced by operating M1 with a small overdrive voltage, which reduces the ΔV_{ov1} term.

The frequency response of the two-stage OTA is compensated using the Miller capacitance C_{c}. The compensation capacitor splits the poles generating a dominant pole [25]. However, the compensation capacitor also creates a right half-plane zero that can degrade the frequency response and cause the amplifier to have a negative phase margin and become unstable. Transistor M7 corrects this problem, creating a resistance that can be used to move the zero to higher frequencies. With the resistance, the location of the zero is

$$z = \frac{1}{\left(\frac{1}{g_{\mathrm{m2}}} - R_{\mathrm{z}} \right) C_{\mathrm{c}}} \tag{4.45}$$

By operating M7 in the linear region, as a resistor, the zero can be moved to infinity if the resistance is equal to $1/g_{\mathrm{m2}}$. This is accomplished by making M7 identical to M2 and operating it with the same gate-source voltage. By doing this, the negative effect of the zero on the frequency response and phase margin can be eliminated. After compensation and zero cancellation the poles of the two-stage OTA are

$$p_1 = \frac{-1}{R_1\left(C_1 + C_{\mathrm{c}}\right) + R_2\left(C_2 + C_{\mathrm{c}}\right) + g_{\mathrm{m2}}R_2R_1C_{\mathrm{c}}} \tag{4.46}$$

$$p_2 = \frac{-g_{\mathrm{m2}}C_{\mathrm{c}}}{C_1C_2 + C_{\mathrm{c}}\left(C_1 + C_2\right)} \tag{4.47}$$

$$p_3 = \frac{-1}{R_{\mathrm{z}}C_1} \tag{4.48}$$

where R_1 is the output resistance of the first stage, R_2 is the output resistance of the second stage, C_1 is the total capacitance connected to the gate of M2 and C_2 is the total capacitance connected to the output node. The first two poles determine the majority of the frequency response and set the phase margin, while the third pole is at a very high frequency and typically has little effect.

The noise of the two-stage OTA is determined primarily by the transistors in the first stage of the amplifier. The noise analysis can be simplified to the circuit shown in Figure 4.18. The circuit is a differential half-circuit that includes only the input transistor M1 and the first stage current source load transistor M3. Together the noise contributions of these two devices dominate the noise performance of the two-stage OTA.

The noise generated by a MOSFET can be divided into two parts. The first is thermal noise and the second is $1/f$ noise. The full expression for the drain current noise of a MOSFET is

$$\overline{i_{\mathrm{d}}^2} = 4kT\gamma g_{\mathrm{m}}\Delta f + \frac{K_{\mathrm{f}}}{C_{\mathrm{ox}}}\frac{g_{\mathrm{m}}^2}{WL}\frac{\Delta f}{f} \tag{4.49}$$

where the first term represents the thermal noise and the second term represents the $1/f$ noise [42]. In the thermal noise k is the Boltzmann constant, T is temperature, γ is a device dependent coefficient, g_{m} is the transconductance of the device and Δf

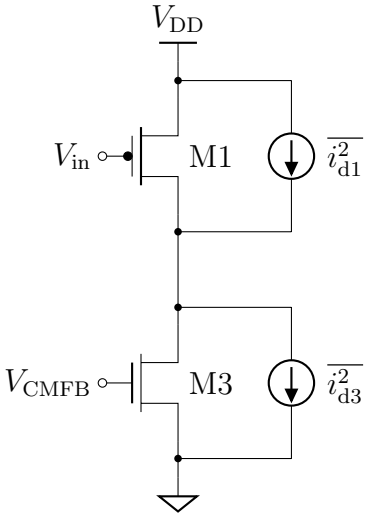


Figure 4.18: Simplified schematic of the OTA for noise analysis.

is the bandwidth over which the noise is being computed. In the $1/f$ noise term K_{f} is a technology dependent coefficient, C_{ox} is the oxide capacitance, W is the width of the device, L is the length of the device and f is frequency.

Using the expression above for the drain current noise power of a MOSFET, the input referred noise voltage and input referred noise current of the two-stage OTA can be calculated. The analysis is performed separately for thermal noise and $1/f$ noise. The input referred thermal noise voltage is

$$\overline{v_{\mathrm{i,thermal}}^2} = 8kT\frac{\gamma_{\mathrm{p}}}{g_{\mathrm{m1}}}\left(1+\frac{\gamma_{\mathrm{n}}}{\gamma_{\mathrm{p}}}\frac{g_{\mathrm{m3}}}{g_{\mathrm{m1}}}\right)\Delta f \tag{4.50}$$

The thermal noise voltage can be reduced by increasing the transconductance of M1, which is accomplished by increasing the bias current. It can also be reduced by ensuring that the $g_{\mathrm{m3}}/g_{\mathrm{m1}}$ ratio is small. This is done by making the channel length of M3 longer than M1. The additional factor of two in the expression comes from the fact that the OTA is a differential circuit. The input referred $1/f$ noise voltage can be calculated using the same method, which results in

$$\overline{v_{\mathrm{i},1/f}^2} = 2\left(\frac{K_{\mathrm{fp}}}{C_{\mathrm{ox}}}\frac{1}{W_1L_1}+\frac{K_{\mathrm{fn}}}{C_{\mathrm{ox}}}\frac{1}{W_3L_3}\frac{g_{\mathrm{m3}}^2}{g_{\mathrm{m1}}^2}\right)\frac{\Delta f}{f} \tag{4.51}$$

The $1/f$ noise voltage can be reduced by increasing the area of M1 and M3. Similar to the thermal noise, the $1/f$ noise voltage can also be reduced by reducing the g_{m3}/g_{m1} ratio.

The input referred current noise can be calculated for the two-stage OTA using a similar procedure. The input referred thermal noise current is

$$\overline{i^2_{i,thermal}} = 2qI_{G1}\Delta f + 4kT\omega^2 C^2_{gs1}\frac{\gamma_p}{g_{m1}}\left(1+\frac{\gamma_n}{\gamma_p}\frac{g_{m3}}{g_{m1}}\right)\Delta f \tag{4.52}$$

where q is the charge of an electron (1.6×10^{-19}), I_{G1} is the gate current of M1, ω is the frequency in radians per second and C_{gs1} is the gate source capacitance of M1. The first term in the expression is technically shot noise, not thermal noise, but it is included here for completeness. The shot noise of a CMOS amplifier is typically negligible because the gate current of a MOSFET is very small (typically less than 1×10^{-15} A). The second term in the input referred current noise is the result of thermal noise. It is usually only significant at very high frequencies because it scales with the square of the frequency. In the event that it is significant in this design, it can be reduced by increasing the transconductance of M1 or by reducing the g_{m3}/g_{m1} ratio. It is important to note that there is no additional factor of two when calculating the input referred current noise of a differential circuit. The input referred $1/f$ noise current is

$$\overline{i^2_{i,1/f}} = \omega^2 C^2_{gs1}\left(\frac{K_{fp}}{C_{ox}}\frac{1}{W_1L_1}+\frac{K_{fn}}{C_{ox}}\frac{1}{W_3L_3}\frac{g^2_{m3}}{g^2_{m1}}\right)\frac{\Delta f}{f} \tag{4.53}$$

The input referred $1/f$ noise current also scales with frequency. Similar to the input referred $1/f$ noise voltage, it can be reduced by using large devices and by reducing the g_{m3}/g_{m1} ratio.

The DC output voltage of the fully-differential two-stage OTA is not well defined, which creates the need for a circuit to regulate this voltage. A common-mode feedback circuit is used for this purpose. The common-mode feedback circuit used in this design is shown in Figure 4.19. The circuit can be divided into two parts. The first part is the common-mode detector, which measures the DC output voltage of the OTA. The common-mode detector is implemented with the two R_{CM} resistors. These resistors

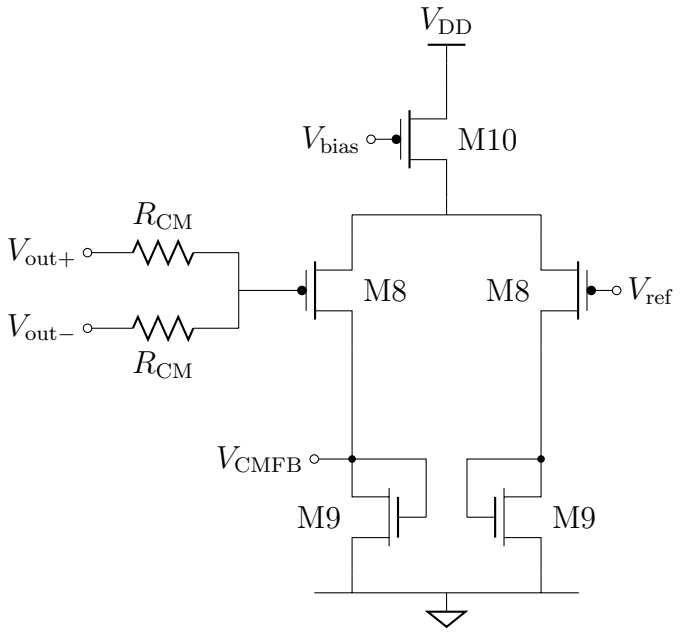


Figure 4.19: Schematic of the common-mode feedback circuit.

essentially calculate the average of the positive and negative outputs of the OTA. The resistors are given a value that is much larger than the output impedance of the OTA to ensure that they don't affect the gain. The second part of the common-mode feedback circuit is the error amplifier, which compares the DC output voltage of the OTA with the desired value, V_{ref}, and amplifies the difference. The output of the error amplifier is fed back to the OTA at the gate of the M3 transistors. This process creates a negative feedback loop that keeps the DC output voltage fixed at the desired value (V_{ref}). This particular common-mode feedback circuit was selected primarily because it doesn't limit the output swing of the OTA, which can be problematic with other common-mode feedback circuits.

The slew rate of the two-stage OTA depends on both stages of the amplifier circuit. As a result, the analysis can be divided into the internal slew rate and the external slew rate. The internal slew rate is

$$SR_{\text{int}} = \frac{2I_{\text{D1}}}{C_{\text{c}}} \tag{4.54}$$

where I_{D1} is the bias current of M1 and C_c is the compensation capacitor. The internal slew rate arises because of the need to charge and discharge the compensation capacitor. The external slew rate is

$$SR_{ext} = \frac{2I_{D4}}{(C_L + C_c)} \tag{4.55}$$

where I_{D4} is the bias current of M4 and C_L is the load capacitance at the output of the OTA. The external slew rate is the slew rate of the output stage of the OTA and is caused by the need to charge and discharge the load capacitance and compensation capacitance. The overall slew rate of the two-stage OTA is the minimum of the internal and external slew rates. It can be increased by increasing the bias currents, at the expense of power dissipation.

The preceeding analysis covers the fully-differential two-stage OTA, which is used in both the LNA and ADC. Additionally, a single-ended version of the circuit is used in the gain stage of the LNA. Figure 4.20 shows the single-ended version of the two-stage Miller compensated OTA circuit. The primary difference is that only one output stage is included and no common-mode feedback circuit is necessary. Most of the design equations for the fully-differential version of the amplifier also apply to the single-ended amplifier.

4.3.3 Design Methodology

The design equations outlined in the previous section are used to guide the design of the two-stage OTAs that are used in the receiver. Each of the OTAs in the receiver has a different set of design goals. For example, some amplifiers require high gain, some require high speed, and others require low noise. Given the number of unique OTAs that need to be designed, an efficient design methodology is needed to quickly arrive at designs that achieve the performance goals.

One common issue with directly using the design equations derived from the small-signal model of the amplifier is that the hand calculations often give very different results than a circuit simulator. This is caused by the fact that the square law model for MOSFETs doesn't always match well with the complex simulation models. This

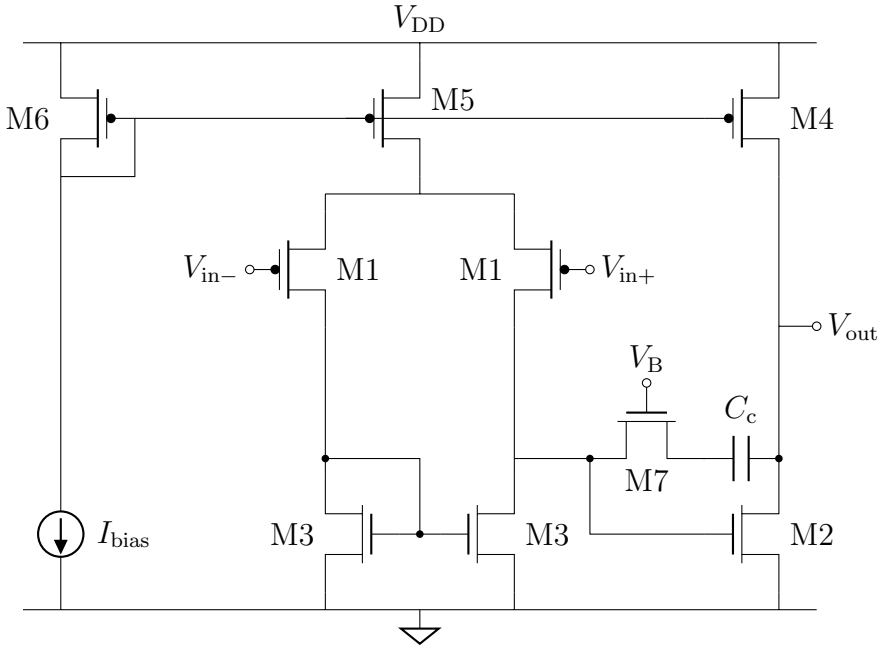


Figure 4.20: Schematic of the single-ended two-stage OTA.

problem is particularly pronounced for short-channel devices. To overcome this problem the $g_{\mathrm{m}}/I_{\mathrm{D}}$ design methodology has been applied [33]. To use this method, first the NMOS and PMOS transistors are characterized. This is accomplished by creating a test-bench with a single PMOS and NMOS transistor and sweeping them over their full range of operating points. At each operating point the relevant transistor parameters are logged in design tables. These parameters include things like the transconductance, bias current, threshold voltage, output resistance, parasitic capacitances and noise coefficients. There are several ways to organize this data, but one popular method is to organize it as a function of the ratio $g_{\mathrm{m}}/I_{\mathrm{D}}$. Although it's not obvious, this is a beneficial organization because the $g_{\mathrm{m}}/I_{\mathrm{D}}$ ratio is directly related to the transistor characteristics. For instance, a small $g_{\mathrm{m}}/I_{\mathrm{D}}$ ratio leads to fast transistors, while a large $g_{\mathrm{m}}/I_{\mathrm{D}}$ ratio leads to high efficiency or low-power transistors. Now when designing, instead of calculating parameters using the square law models, the parameters can be found by looking them up in the design tables. The matching between predicted performance and simulation results is greatly improved by using parameters from the design tables.

The basic methodology used to design the OTAs involves two steps. First, the design is iterated in MATLAB to arrive at a set of amplifier parameters (transistor sizes and bias currents) that meet the design specifications for that particular amplifier. The basic inputs for the iterative design are the transconductance of each transistor, the channel length of each transistor and the $g_{\mathrm{m}}/I_{\mathrm{D}}$ value for each transistor. The amplifier performance is predicted using the design equations derived in Section 4.3.2 and the design tables are used to look up the transistor parameters. Once a design that meets the specifications is found, the second step involves simulating the design at the transistor-level to verify that the predicted performance matches with simulation results. The simulations verify that the approximations made in the design equations are valid and that the amplifier performs as expected.

This design approach allows for much smarter and more efficient design because the design equations show the most important knobs that can be tuned to achieve the desired performance goals, rather than blindly changing parameters in the circuit until the design works. Further, the $g_{\mathrm{m}}/I_{\mathrm{D}}$ design methodology ensures good matching between hand calculations and simulation results.

4.4 Receiver Implementation

4.4.1 Overview

The top-level receiver architecture consists of the interconnection of the LNA and the ADC. Thanks to the implicit anti-alias filtering of the continuous-time delta-sigma modulator, no additional filtering is required. The full receiver schematic is shown in Figure 4.21. The input of the receiver is a fully-differential signal that originates at the antenna and is connected to the receiver with the transformer. The output of the receiver consists of two digital signals from the ADC, which are the 1-bit digital output data stream and the 15 MHz clock output.

In addition to the primary input and output signals, the receiver has a number of control signals. The LNA has three control signals: an external bias voltage that is used to optionally bias the LNA input stage, a bias mode selection signal that

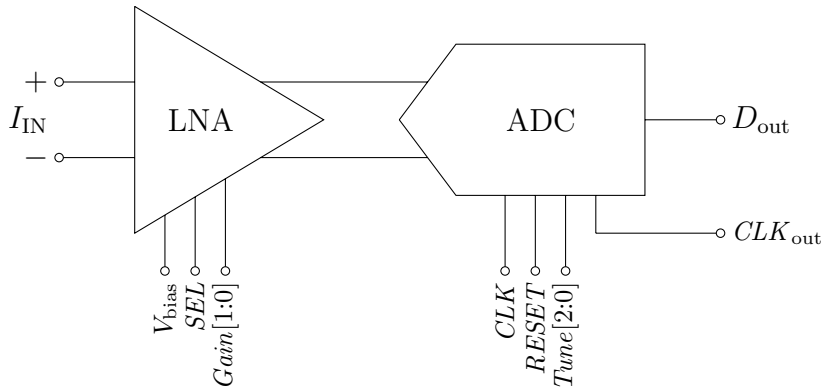


Figure 4.21: Block diagram of the receiver.

selects between either automatic biasing or manual biasing, and a 2-bit gain selection signal that selects between the four LNA gain modes. In addition, the ADC has three control signals: a 15 MHz square wave clock signal, a reset signal that clears the RC integrators, and a 3-bit RC tuning signal that adjusts the capacitors to compensate for process variation.

4.4.2 Biasing

For the purpose of validating the performance of the receiver in the lab, a simplistic biasing architecture could have been employed. For example, a lab current source could have been used to provide the reference current. However, the goal for the single-chip receiver was to design a system that was robust enough to be deployed in the field without further modification. To satisfy this goal an on-chip biasing network was designed that could withstand changes in process, voltage and temperature.

A constant-g_{m} current source was selected to provide the bias currents for the OTAs and the other active circuits in the receiver [34]. The schematic of the constant-g_{m} current source is shown in Figure 4.22. The output bias current of the constant-g_{m} current source is

$$I_{\text{bias}} = \frac{V_{\text{ov1}}}{R_{\text{ref}}}\left(1 - \frac{1}{\sqrt{m}}\right) \tag{4.56}$$

where V_{ov1} is the overdrive voltage of M1, R_{ref} is an off-chip reference resistor and m is the scaling ratio between transistors M2 and M1. While this may not seem

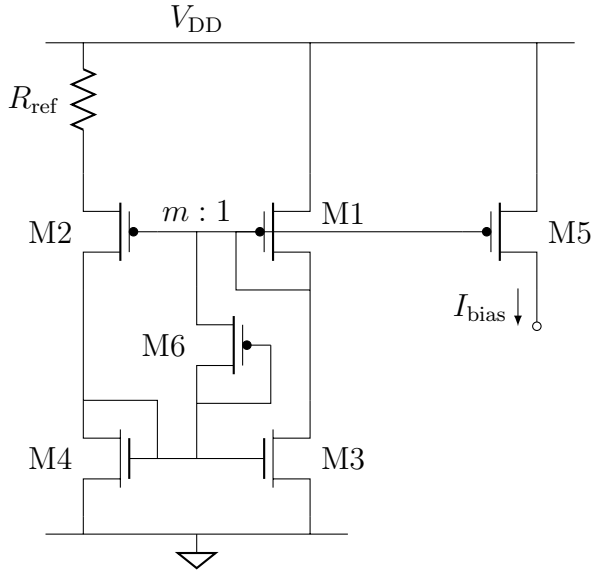


Figure 4.22: Schematic of the constant-g_{m} current source.

very useful, when the transconductance is calculated it becomes more clear. The transconductance of transistor M1 is

$$g_{\mathrm{m1}} = \frac{2}{R_{\mathrm{ref}}}\left(1 - \frac{1}{\sqrt{m}}\right) \tag{4.57}$$

The transconductance depends only on the reference resistor and the scaling ratio. This means that any transistor biased with this reference current will have the same transconductance independent of changes in process, voltage or temperature. Given that the noise of the OTAs depends directly on the transconductance of the input devices, the constant transconductance characteristic will provide predictable noise performance regardless of the operating conditions. Transistor M6 in the circuit is a diode connected MOSFET that ensures that the self-biased feedback loop starts up correctly when power is applied to the current source.

4.4.3 Noise Coupling

The coupling of noise between the various circuits on an integrated circuit is often a challenging design problem [23, 46]. In this receiver design it is particularly important

as noise generated by the ADC could corrupt the sensitive LNA. In fact, this is part of the reason that in past VLF receiver designs the LNA was separated from the noisy digital portion of the receiver by placing them in separate enclosures with a long cable between them. Three different strategies have been used to reduce the amount of on-chip noise coupling in the single-chip receiver.

First, differential signaling has been used throughout the receiver design. All signal path connections are fully-differential, from the LNA input through to the delta-sigma ADC output. Differential signaling is much more robust to noise than single-ended signals assuming that the circuits are matched and have a good common-mode rejection ratio (CMRR).

Second, separate supplies are used for the various circuit blocks in the design. This ensures that noise does not couple through the power or ground rails. There are five different supplies used in the single-chip receiver: LNA analog supply, ADC analog supply, ADC digital supply, ADC reference supply and ESD protection supply. Each supply consists of a power and ground connection that are routed to dedicated pins on the chip. Each supply has its own decoupling network on the test board. There are no on-chip connections between the supplies. Further, the LNA and the ADC each have their own reference current source to prevent noise from coupling through the bias network.

Third, the layout is optimized to minimize noise coupling. The two main circuit blocks, the LNA and the ADC, are physically separated on the die by approximately 60 µm to prevent noise coupling through the substrate. Within the ADC, the noisy digital circuits are placed away from sensitive analog circuits and sensitive interconnect is not run near noisy signals. The pin locations have been carefully selected to ensure that noisy digital signals are not near the sensitive LNA input signals. Guard rings are also used throughout the layout to locally isolate sensitive circuits and prevent noise from coupling out of noisy circuits [29].

4.5 Chip Layout

The single-chip receiver was fabricated in a 0.13 µm BiCMOS technology from Texas Instruments. A photograph of the die is shown in Figure 4.23. The die area is 2.56 mm^2 (1.6 mm $\times$ 1.6 mm). The large rectangular block on the right half of the die is the ADC. The large rectangular block on the left half of the die is the LNA. There are also two smaller test circuit blocks visible just above the LNA.

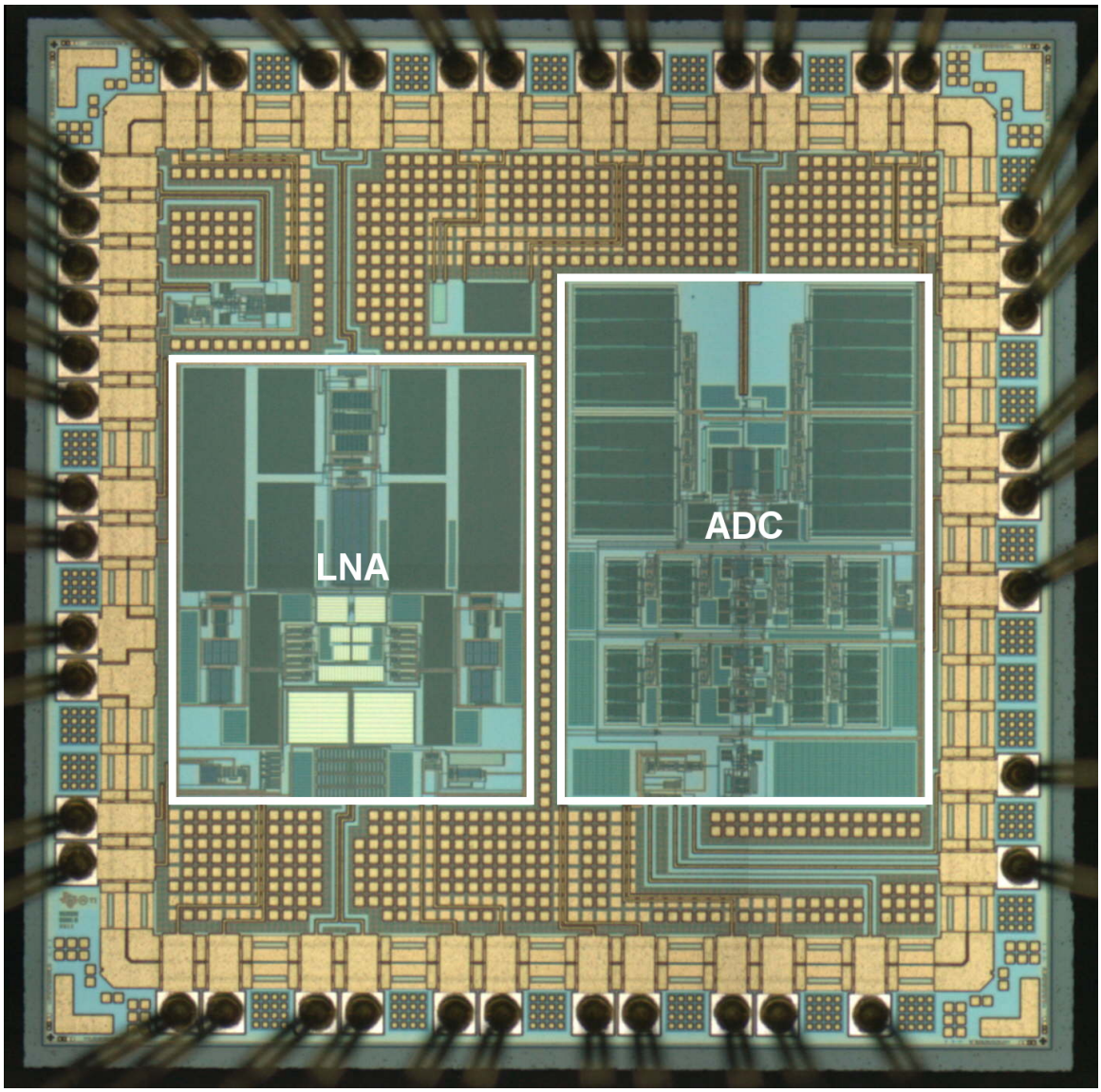


Figure 4.23: Die photo of the single-chip receiver.

Chapter 5

Measurement Results

This chapter presents the measurement results for the single-chip VLF magnetic field receiver. In addition to testing the full receiver, the LNA and ADC are each tested individually. The results are divided into four sections with each section describing the test setup and corresponding measurements. The first section examines the performance of the LNA, which includes measurements of the frequency response, sensitivity, linearity and power dissipation. The second section covers the ADC performance, which includes the dynamic performance, anti-alias filtering and power dissipation. The third section presents the results of the full receiver, which includes the dynamic performance, noise coupling, anti-alias filtering and power dissipation. Finally, the fourth section details field test results that were collected at two VLF antenna sites. This final section also compares the field test data with data from the AWESOME receiver.

A custom printed circuit board (PCB) was designed to test the single-chip receiver. A picture of the finished PCB is shown in Figure 5.1. The single-chip receiver is visible near the center of the board. It was packaged in a 48-pin quad flat no-lead (QFN) package that is roughly 7 mm $\times$ 7 mm. The hand-wound 24:548 center-tapped transformer is also visible on the test board. To prevent coupling between traces on the PCB, care was taken during design to physically separate the noisy digital signals from the sensitive analog signals. Further, all of the differential signals are routed side-by-side with length-matched traces to ensure that any noise that does couple

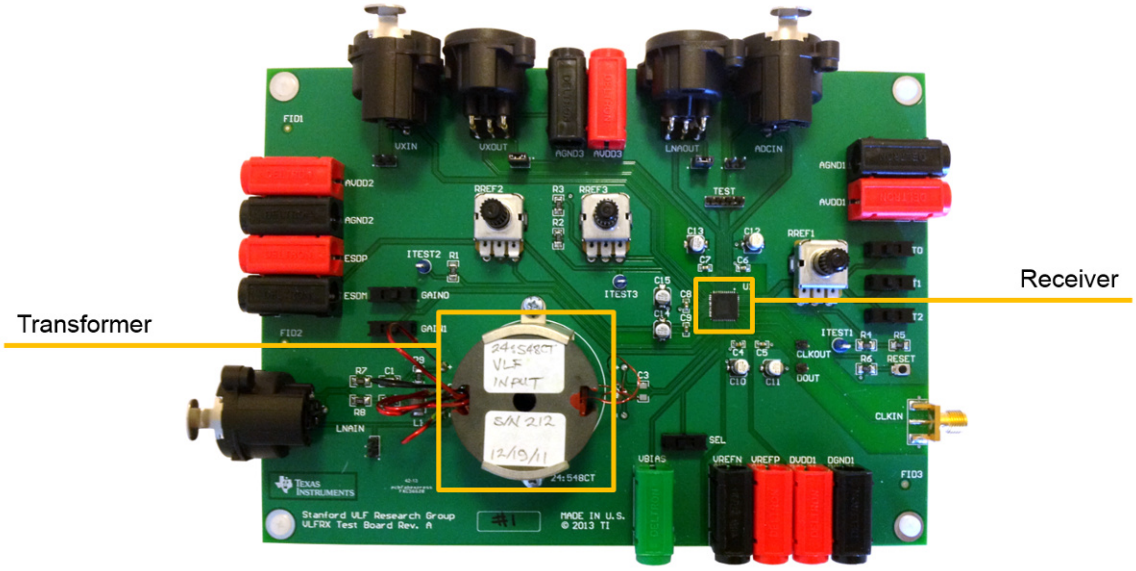


Figure 5.1: Test board for the single-chip receiver.

into these lines will appear as a common-mode signal, which is then rejected by the differential circuits in the receiver.

5.1 LNA Measurement Results

5.1.1 Test Setup

The test setup used to measure the LNA performance is shown in Figure 5.2. The input signal for the LNA was generated with a Stanford Research Systems SR-1 Audio Analyzer. The SR-1 was selected primarily for its ability to generate low-distortion signals. The instrument is capable of generating a sinusoidal signal with a SFDR of approximately 105 dB over the entire receiver bandwidth (300 Hz to 50 kHz). This level of distortion is well below the 90 dB SFDR performance target of the receiver, which means that the input signal from the SR-1 will not limit the SFDR of the system and no additional filtering of the input signal is required. The SR-1 generates a fully-differential signal. The analog output port on the SR-1 was connected to the injection circuit on the test board with a shielded XLR cable to reduce the amount

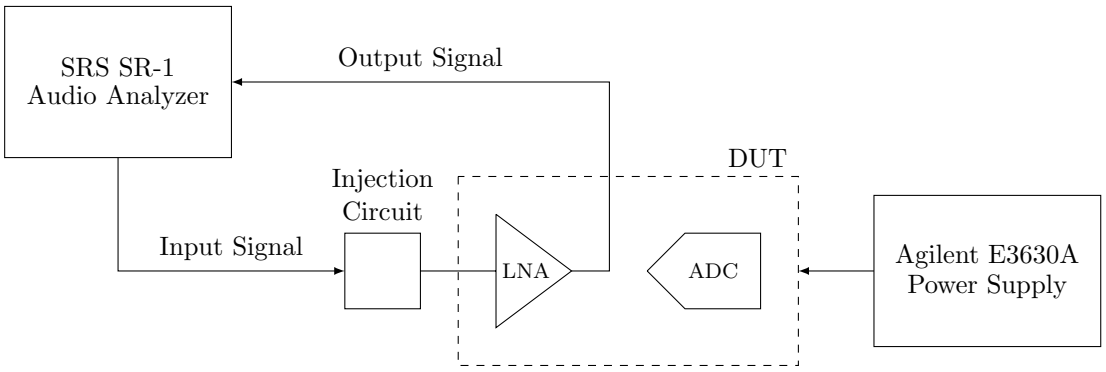


Figure 5.2: Test setup for LNA measurements.

of noise coupling into the input of the LNA.

The injection circuit interfaces between the signal generator and the LNA and is used to inject a test current in parallel with a dummy antenna as described in Section 2.1.5. It consists of three main components. The first component converts the differential voltage from the SR-1 into a current using a passive RC network. The second component is a dummy antenna that is implemented with a 1 Ω resistor and a 1 mH inductor. The dummy antenna mimics the impedance of an actual antenna. The third component is the 24:548 center-tapped input transformer, which matches the input impedance of the LNA to the impedance of the antenna. The injection circuit components are represented with a single block in the test setup diagram.

The fully-differential output of the LNA was connected to the analog input port on the SR-1 via a shielded XLR cable. The SR-1 was configured to compute the spectrum of the signal, which enabled monitoring of the signal amplitude, noise floor, harmonics and other performance metrics in real-time. Additionally, the SR-1 provided a 100 kΩ load impedance. This impedance is roughly equivalent to the ADC input impedance, which ensures that there is a good match between the LNA measurements and the performance of the LNA when it is used in the full receiver system.

Power was supplied to the device under test (DUT) by an Agilent E3630A Triple Output DC Power Supply. Separate supply and ground connections were used to power the LNA and the ESD protection circuitry. Separate supplies are not necessary for the LNA measurements, but are important for ADC and receiver measurements

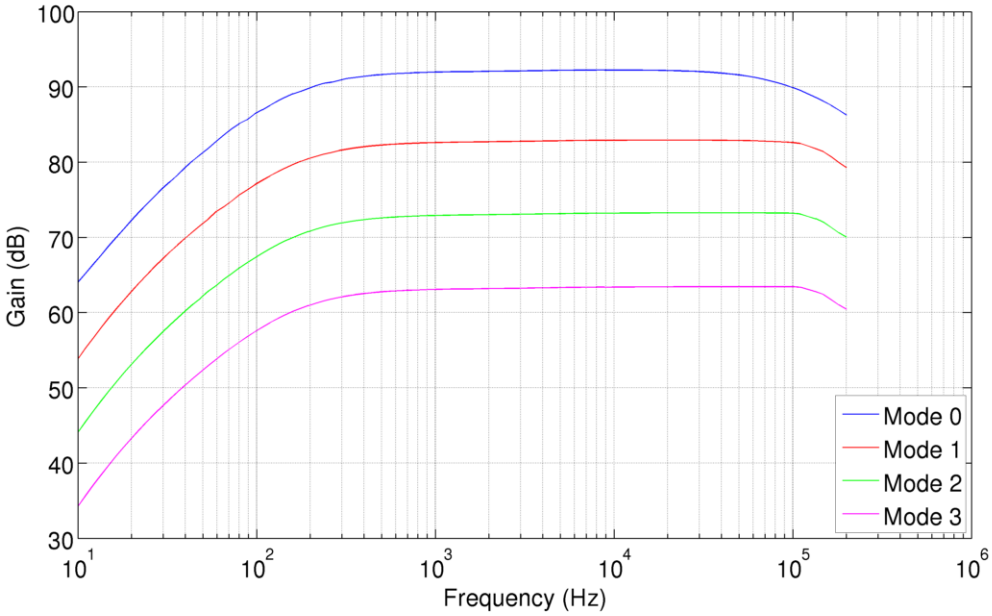


Figure 5.3: LNA frequency response.

to reduce noise coupling between the various circuit blocks. All components of the receiver run on 1.2 V. Unless otherwise noted, all of the measurements use the auto-bias setting for the LNA. In this setting the input stage bias voltage is set by the automatic biasing system, not by an external reference voltage.

5.1.2 Frequency Response

The frequency response of the LNA was measured by configuring the signal generator to sweep over its entire frequency range (10 Hz to 200 kHz) and calculate the ratio of the output amplitude to the input amplitude at each test frequency. The results are shown in Figure 5.3. The horizontal axis corresponds to the frequency of the test signal and the vertical axis is the gain in dB. The gain includes the effect of the input transformer, which means that it is the gain from the current generated by the loop antenna to the voltage at the LNA output. Therefore, it is the gain of the full front-end of the receiver.

The frequency response figure includes curves for all four LNA gain modes. The

modes are separated by roughly 10 dB. Mode 0, the highest gain mode, has a peak gain of 92.25 dB. Mode 1 has a peak gain of 82.93 dB. Mode 2 has a peak gain of 73.26 dB. Mode 3, the lowest gain mode, has a peak gain of 63.44 dB. The gain can also be referred to the magnetic field at the antenna if the antenna parameters are known. With a six-turn 4.9 meter square antenna, the gain of the front-end is 5.91 mV/pT in mode 0, 2.02 mV/pT in mode 1, 0.66 mV/pT in mode 2 and 0.21 mV/pT in mode 3.

The transimpedance of the LNA can be calculated by adjusting for the effect of the transformer. The current gain of the 24:548 transformer is approximately -27.17 dB. The effect of the transformer can be removed by adding this value back to the peak front-end gain values from Figure 5.3. The resulting transimpedance values for the four gain modes are 119.42 dB, 110.10 dB, 100.43 dB and 90.61 dB. The goal for the LNA transimpedance was 100 dB, which means that the four gain modes enable the end-user to select from a range of gain values that extends above and below the target value.

The bandwidth of the LNA is also an important performance metric. The design goal was for the receiver bandwidth to extend from 300 Hz to 50 kHz. The 3 dB bandwidth of the LNA is calculated from the frequency response. The antenna impedance causes the gain to roll-off at low frequencies. The antenna is unchanged between the gain modes so the roll-off should be the same in all cases. As expected, the 3 dB point is approximately 170 Hz in all of the gain modes. Roll-off at the high-end of the frequency range is caused by the poles of the LNA, which are not necessarily the same between gain modes. For this reason, it is expected that the high frequency roll-off will occur at a different frequency in each gain mode. In the highest gain mode, mode 0, the 3 dB point is at 117.18 kHz. In mode 1 the 3 dB point is at 182.03 kHz. In mode 2 it's at 191.94 kHz and in mode 3 it's at 199.30 kHz. Although the bandwidth depends on the gain mode, in all cases it comfortably exceeds the 50 kHz design goal.

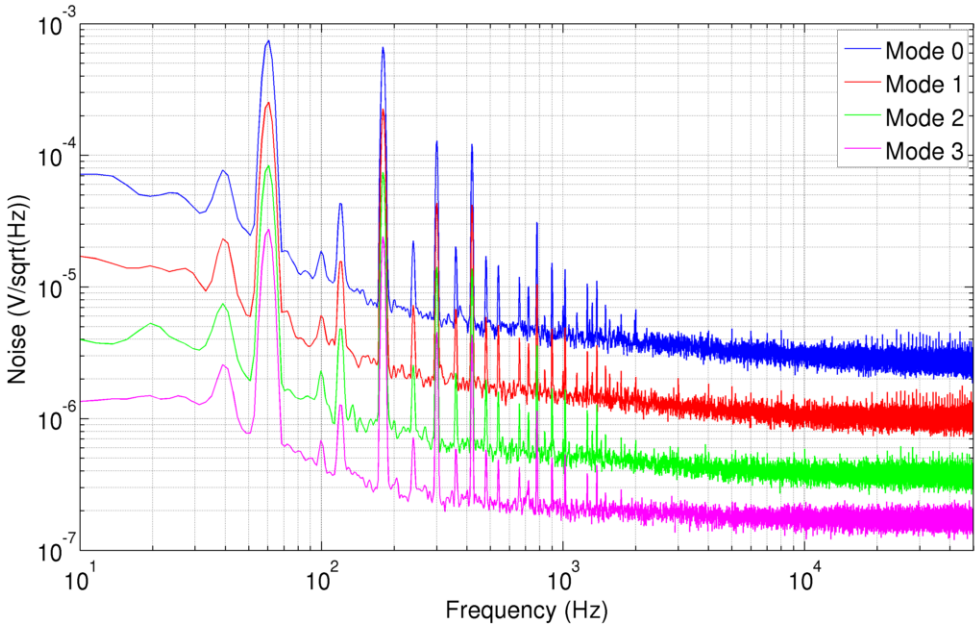


Figure 5.4: LNA output noise spectrum.

5.1.3 Sensitivity

The noise performance of a VLF receiver is characterized in terms of its sensitivity. The sensitivity is defined as the magnetic field amplitude at the antenna that will result in a 0 dB signal-to-noise ratio at the LNA output when measured in a 1 Hz bandwidth [39]. Essentially, the sensitivity is the input amplitude that is equivalent to the noise floor at the LNA output at any given frequency. Smaller values for the sensitivity are better.

The sensitivity can be calculated from the output noise spectrum. The output noise spectrum is measured by removing the input signal from the LNA and capturing the output with the SR-1 Audio Analyzer. The SR-1 then performs an FFT to generate the output spectrum. Figure 5.4 shows the LNA output noise spectrum from 10 Hz to 50 kHz for each gain mode. A data length of 32 thousand samples was used and the result was averaged 16 times to smooth the spectrum. As expected, the noise floor increases as the gain increases because the input stage dominates the noise performance of the LNA.

The spurious tones visible between 10 Hz and 2 kHz are the result of power line noise coupling into the system. The largest tones are visible at 60 Hz, 180 Hz, 300 Hz and 420 Hz, which are the fundamental, 3rd, 5th and 7th harmonic respectively. There are also smaller tones visible at 50 Hz and its harmonics, as well as the even harmonics of 60 Hz. This power line noise is likely coupling into the system at two points. First, through the power supply rails from the E3630A DC Power Supply, which runs on AC power. Second, through radiated electromagnetic interference (EMI) from nearby electronic equipment, which is being captured by the large coil in the input transformer. Fortunately, the power line noise is small enough and at low enough frequency that it does not adversely affect the ability to measure the LNA performance. It is also important to point out that in a real deployment the receiver would run on battery power and would be located at a quiet site far away from any other electronics. Under these conditions power line noise would not be a concern. For the purpose of calculating the sensitivity of the LNA, the power line noise is filtered out in post-processing and a best-fit line is computed.

The first step to compute the sensitivity of the LNA is to calculate the input referred noise. This is done by dividing the output noise spectrum by the gain of the LNA. The input referred noise is then converted into an equivalent magnetic field amplitude at the antenna to determine the sensitivity. A six-turn 4.9 meter square antenna was used for this calculation. The resulting sensitivity is shown in Figure 5.5 for each gain mode.

The sensitivity is below 1 $\mathrm{fT/Hz^{1/2}}$ over the entire target bandwidth (300 Hz to 50 kHz) in all four gain modes. The LNA has a minimum sensitivity of 0.240 $\mathrm{fT/Hz^{1/2}}$ in mode 0, 0.250 $\mathrm{fT/Hz^{1/2}}$ in mode 1, 0.282 $\mathrm{fT/Hz^{1/2}}$ in mode 2 and 0.398 $\mathrm{fT/Hz^{1/2}}$ in mode 3. These results are consistent with Equation 4.17, which predicted that the noise would increase slightly in the lower gain modes due to the larger resistors that are switched into the gain stage.

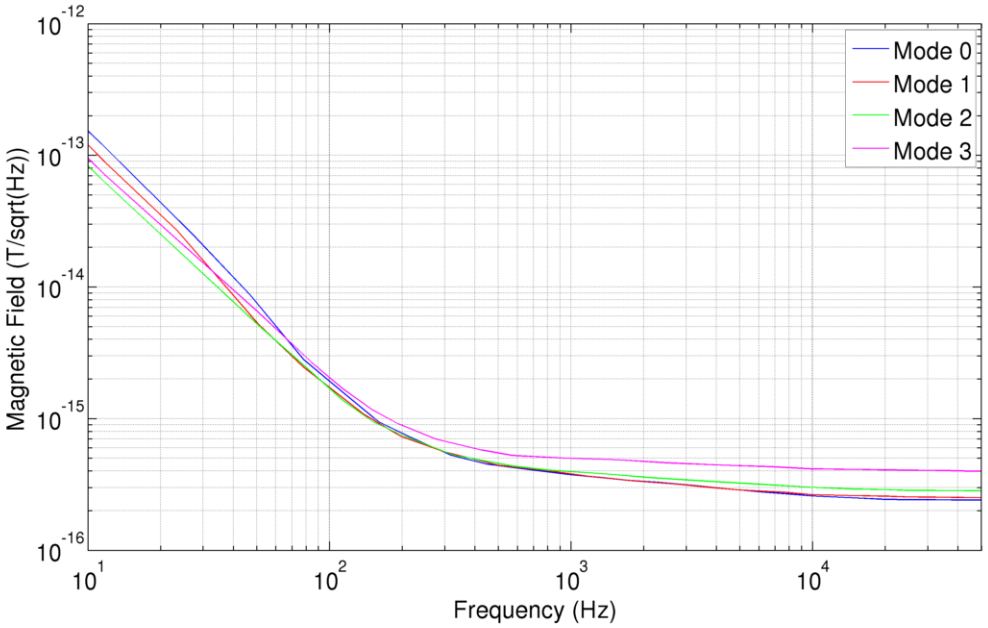


Figure 5.5: LNA sensitivity.

5.1.4 Linearity

The linearity of the LNA is characterized by the peak spurious-free dynamic range (SFDR). The SFDR is defined as the ratio of the input signal to the strongest spurious signal, which is typically a harmonic of the input signal. For the purpose of determining the SFDR, the power line noise seen in Figure 5.4 is not included in the calculation.

To determine the peak SFDR the input signal is swept over a range of amplitude values. Figure 5.6 shows the amplitude sweep for each gain mode. The horizontal axis represents the peak-to-peak voltage applied to the injection circuit. The vertical axis represents the calculated SFDR in dB at the output of the LNA. A 10 kHz input frequency was used because it lies near the middle of the VLF band and because the most important harmonics, the 2nd through the 5th, also fall in-band.

At small input signal amplitudes the SFDR increases linearly with the input amplitude. This is because the harmonics are below the noise floor so the SFDR is simply the ratio between the input signal and the noise floor (the noise floor is constant).

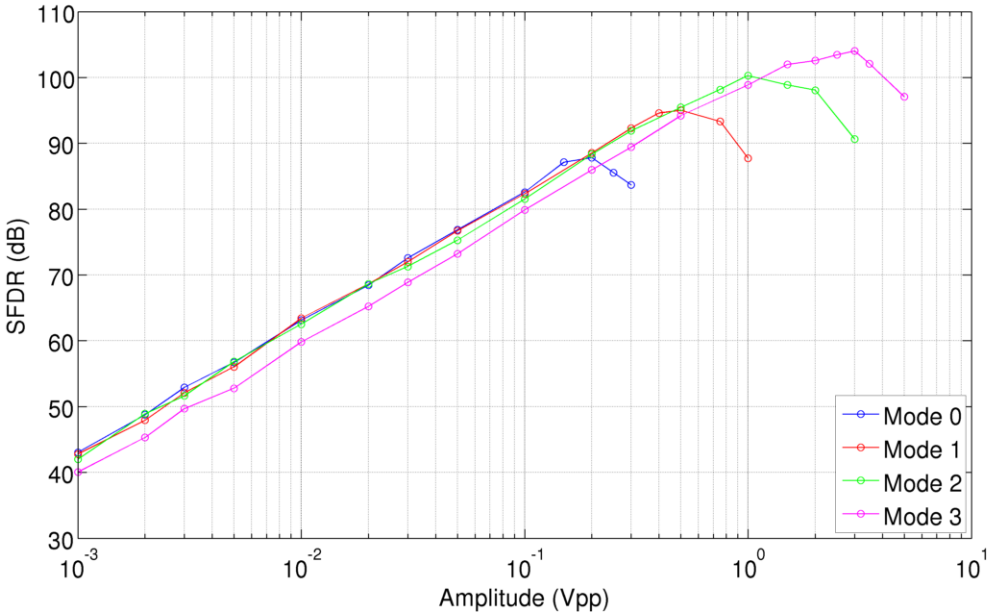


Figure 5.6: LNA SFDR versus input amplitude.

However, as the input signal amplitude increases, eventually it becomes large enough that the harmonics in the LNA output spectrum exceed the noise floor and the plot levels off and ultimately starts decreasing due to the harmonics growing at a faster rate than the fundamental.

The peak SFDR varies depending on the gain mode. The peak SFDR is 87.81 dB in mode 0, 95.01 dB in mode 1, 100.30 dB in mode 2 and 104.02 dB in mode 3. The gain stage in the LNA limits the linearity. The reason that the peak SFDR is different in each mode is because the loop gain of the feedback circuits changes depending on which gain mode is selected. When the gain stage is in a low gain mode the loop gain is high, which results in a higher SFDR. In contrast, when the gain stage is in a high gain mode the loop gain is low, which results in a lower SFDR.

To further illustrate the peak SFDR, an output spectrum for each gain mode was generated using a 10 kHz input signal. The amplitude of the input signal was chosen to be the amplitude that resulted in the maximum SFDR from the corresponding amplitude sweep. The output spectrum that illustrates the maximum SFDR for each gain mode is shown in Figures 5.7 to 5.10.

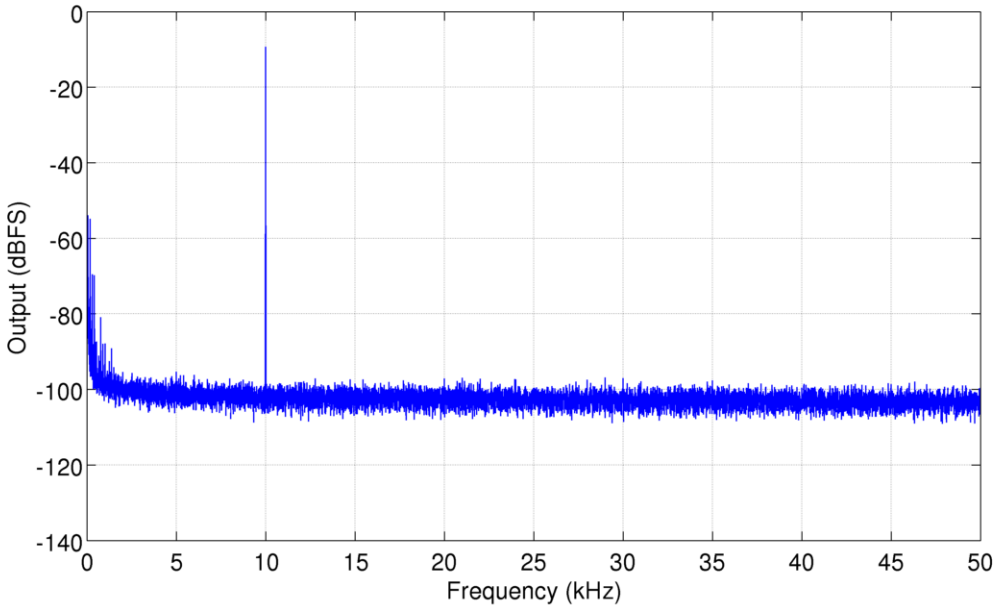


Figure 5.7: LNA output spectrum with the peak SFDR in mode 0.

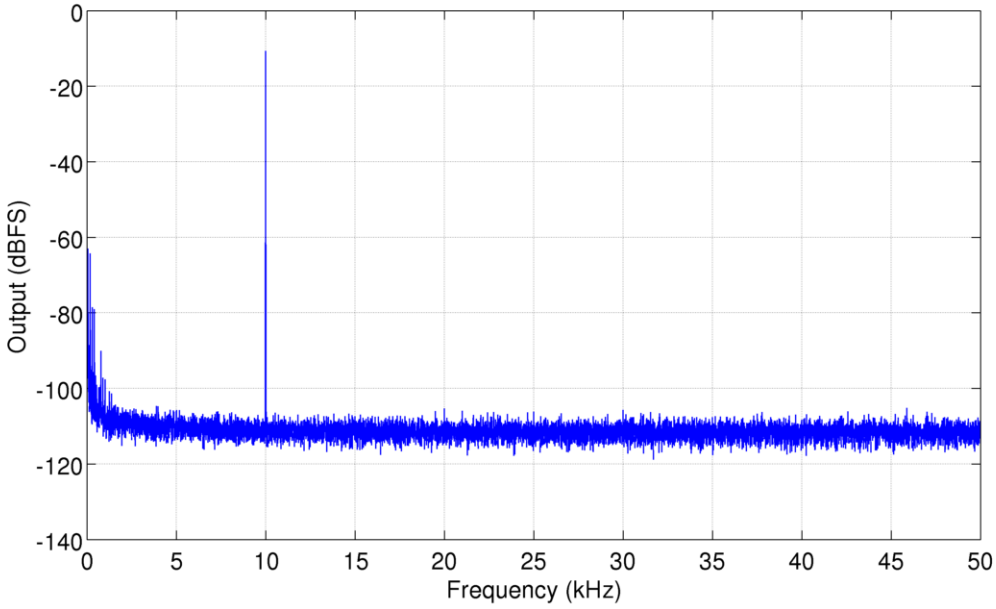


Figure 5.8: LNA output spectrum with the peak SFDR in mode 1.

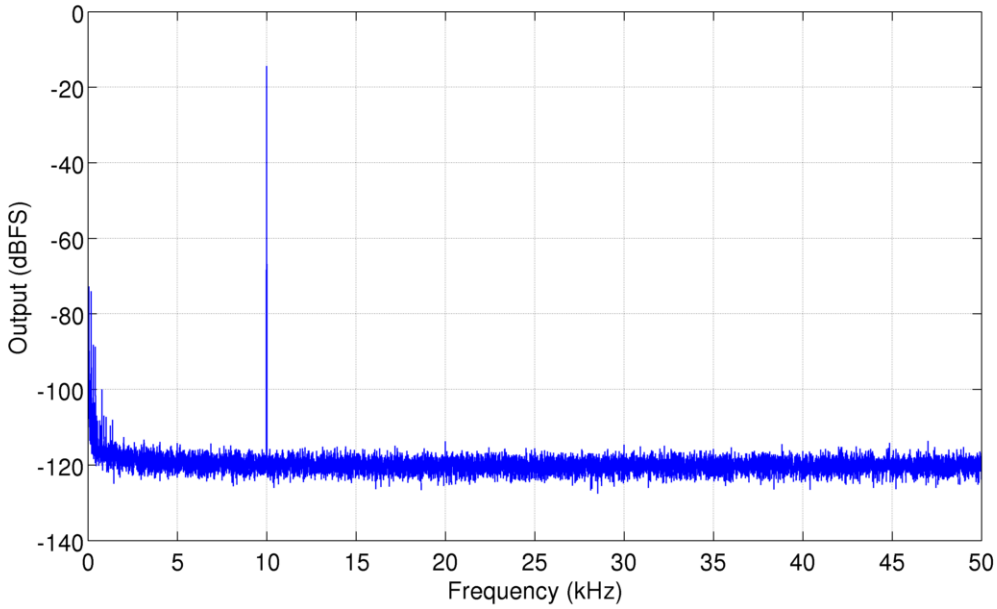


Figure 5.9: LNA output spectrum with the peak SFDR in mode 2.

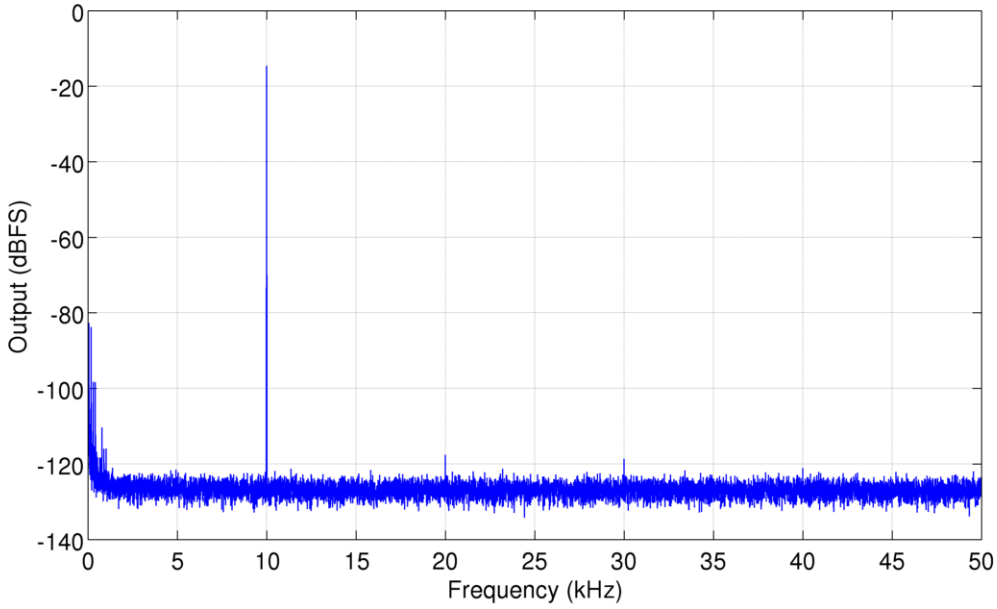


Figure 5.10: LNA output spectrum with the peak SFDR in mode 3.

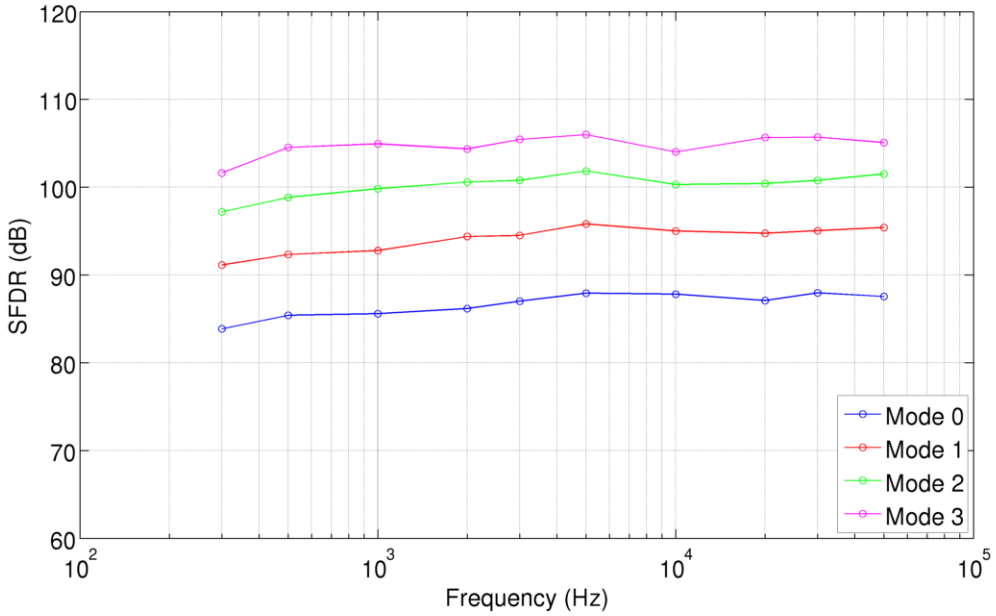


Figure 5.11: LNA SFDR versus input frequency.

Measurements were also taken to verify the linearity of the LNA as a function of the input frequency. To accomplish this the input frequency was swept over the entire amplifier bandwidth, from 300 Hz to 50 kHz. The input amplitude used for each gain mode was the input amplitude that produced the maximum SFDR in the amplitude sweep (Figure 5.6). The results of the frequency sweep are shown in Figure 5.11.

The linearity performance is consistent over the full range of frequencies. In mode 0 the SFDR hovers around 87 dB. In mode 1 the SFDR hovers around 96 dB. In mode 2 the SFDR hovers around 100 dB. In mode 3 the SFDR hovers around 105 dB. There is a small decrease in the SFDR below 1 kHz, but this can be attributed to the roll-off of the amplifier gain at the low-end of the frequency band.

5.1.5 Summary

The LNA includes four modes with gain values ranging from 92.25 dB to 63.44 dB when the effect of the transformer is included. The 3 dB bandwidth extends from approximately 170 Hz to over 100 kHz, with the high frequency cutoff depending on

Table 5.1: LNA measurement results summary.

Measurement	Mode 0	Mode 1	Mode 2	Mode 3
Front-End Gain (dB)	92.25	82.93	73.26	63.44
System Gain (mV/pT)	5.91	2.02	0.66	0.21
Bandwidth Start (Hz)	168.87	170.37	171.39	171.71
Bandwidth End (kHz)	117.18	182.03	191.94	199.30
Sensitivity (fT/Hz$^{1/2}$)	0.240	0.250	0.282	0.398
Peak SFDR (dB)	87.81	95.01	100.30	104.02
Power Dissipation (µW)	907.88	908.60	908.48	908.72

the selected gain mode. The sensitivity is well below the 1 fT/Hz$^{1/2}$ design goal, with a range of 0.240 fT/Hz$^{1/2}$ to 0.398 fT/Hz$^{1/2}$. The linearity of the LNA, which was measured in terms of the peak SFDR, varies from 87.81 dB to 104.02 dB. The power dissipation of the LNA was approximately 908 µW, which was measured using a BK Precision 5492 5 1/2 Digit Multimeter.

Table 5.1 shows a full summary of the LNA measurement results for each gain mode. It is important to point out that a six-turn 4.9 meter square antenna was used in the calculation of the system gain and the sensitivity. Additionally, the peak SFDR values are the maximum values from the amplitude sweep, which was performed with a 10 kHz input signal.

5.2 ADC Measurement Results

5.2.1 Test Setup

The test setup for the ADC measurements is shown in Figure 5.12. Similar to the LNA test setup, the input signal to the ADC is generated by the Stanford Research Systems SR-1 Audio Analyzer. This signal generator was selected for its good distortion performance, which doesn't require any additional filtering. It outputs a fully-differential signal that is fed directly to the ADC input via a shielded XLR cable.

The clock signal for the ADC is provided by an Agilent 81110A Pulse Generator.

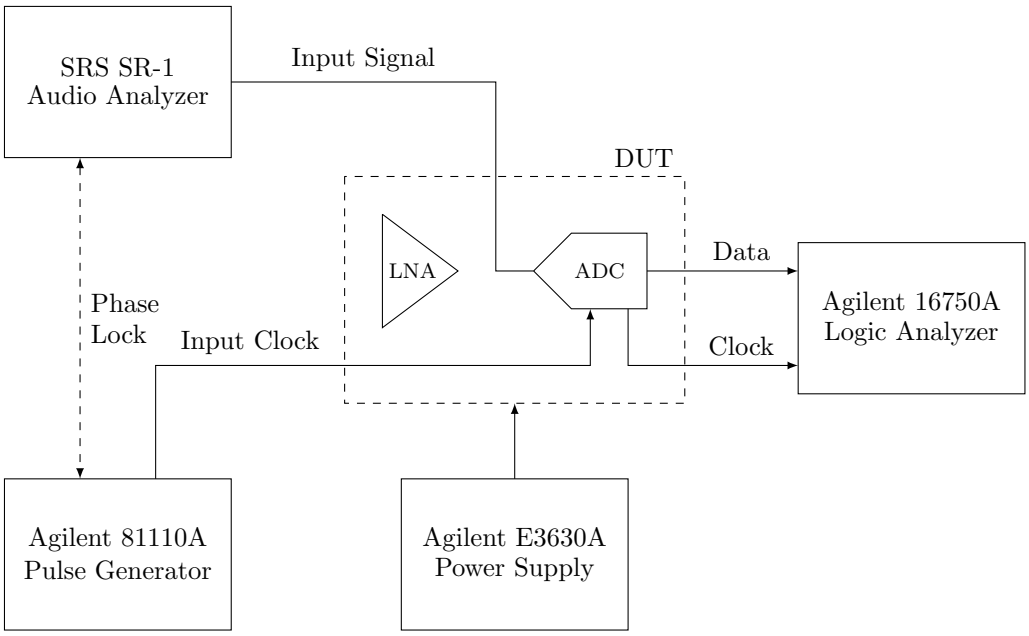


Figure 5.12: Test setup for ADC measurements.

This clock generator was selected for its good jitter performance of roughly 15 psRMS. A clock with a large amount of jitter can degrade the performance of the ADC [12]. The clock generator was configured to output a 1.2 V single-ended square wave at 15 MHz.

In order to produce a clean output spectrum from the ADC it is necessary to prevent spectral smearing. Smearing occurs when the input signal doesn't fall directly into one of the FFT bins. Although FFT windowing can be used to alleviate the problem, it is possible to nearly completely eliminate smearing in a lab environment when precise control of the input signal and clock source is available. This is accomplished by phase-locking the input signal to the clock source [31]. In the ADC test setup this is done by connecting a copy of the 15 MHz clock to the external reference port on the SR-1.

The ADC outputs two digital signals. The first is the 1-bit data stream at 15 MHz. The second is the corresponding 15 MHz clock signal. The digital output signals are captured with an Agilent 16750A Logic Analyzer. The logic analyzer is run in state mode, which means that the data is collected synchronously with the 15 MHz clock

output from the ADC. The resulting data files are stored on the logic analyzer and then transferred to a PC for analysis in MATLAB.

Power for the device under test is provided by an Agilent E3630A DC Power Supply. The setup uses four separate supply connections to power the test chip: ADC analog supply, ADC digital supply, ADC reference voltage and ESD protection supply. Each supply has a separate connection on the test board and its own dedicated ground connection. The supply connections also each have a separate decoupling network to prevent noise coupling. All of the supplies run at 1.2 V.

5.2.2 Output Spectrum

A typical output spectrum from the ADC is shown in Figure 5.13. The horizontal axis represents frequency, which extends from DC to 7.5 MHz ($f_s/2$). The vertical axis is the magnitude of the signal in units of dBFS/NBW. In this particular example a -10 dBFS sinusoidal signal at 10 kHz was input to the ADC. This signal is visible as the large spike near the middle of the output spectrum. In order to prevent spectral smearing, the exact input frequency is actually 10.070801 kHz, which falls exactly in an FFT bin. The 1-bit ADC output bitstream was processed in MATLAB using an appropriately scaled FFT with a Hann window. The data length was 2,097,152 samples.

The noise shaping from the delta-sigma modulator is clearly visible in the spectrum. The majority of the noise in the spectrum is pushed to higher frequencies where it can be subsequently filtered with a digital decimation filter. This is possible because the ADC oversamples the input signal, causing the majority of the noise to be outside the desired 50 kHz band.

There are a few other relevant features of the spectrum that are worth pointing out. The first is the spike at the far left of the spectrum. This peak corresponds to the DC offset of the ADC. The second is the small peak around 60 Hz, which can be attributed to power line noise. Both the DC offset and the 60 Hz noise are not included in the performance calculations of the ADC, such as the spurious-free dynamic range. This is because both of these signals fall below the lower limit of the

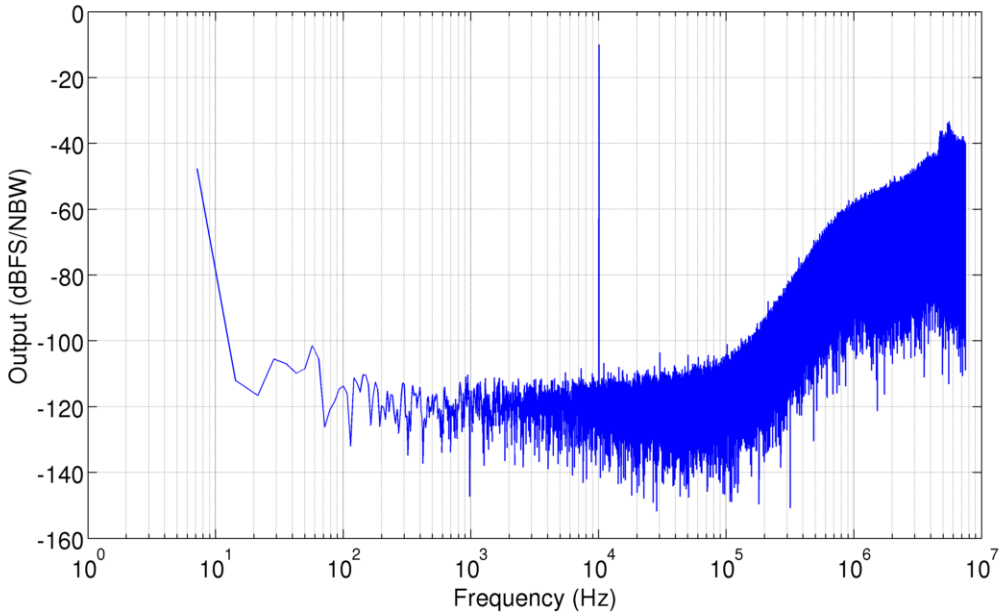


Figure 5.13: ADC output spectrum.

receiver bandwidth (300 Hz). Finally, the 3rd and 5th harmonic of the 10 kHz input signal are also visible in the spectrum at 30 kHz and 50 kHz, respectively.

5.2.3 Dynamic Performance

The performance of an ADC can be characterized using either static performance metrics or dynamic performance metrics. Static performance performance metrics include the gain error, offset, differential nonlinearity (DNL) and integral nonlinearity (INL). Dynamic performance metrics include the signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR) and the spurious-free dynamic range (SFDR). In general, delta-sigma modulators are characterized in terms of dynamic performance metrics [38]. Therefore, dynamic performance metrics are used in this analysis.

By sweeping the input signal amplitude the peak value of the SNR, SNDR and SFDR can be determined. Figure 5.14 shows the amplitude sweep from -80 dBFS to 0 dBFS using a 10 kHz input frequency. The horizontal axis in this plot represents the input amplitude in dB relative to the full-scale range of the ADC. The vertical

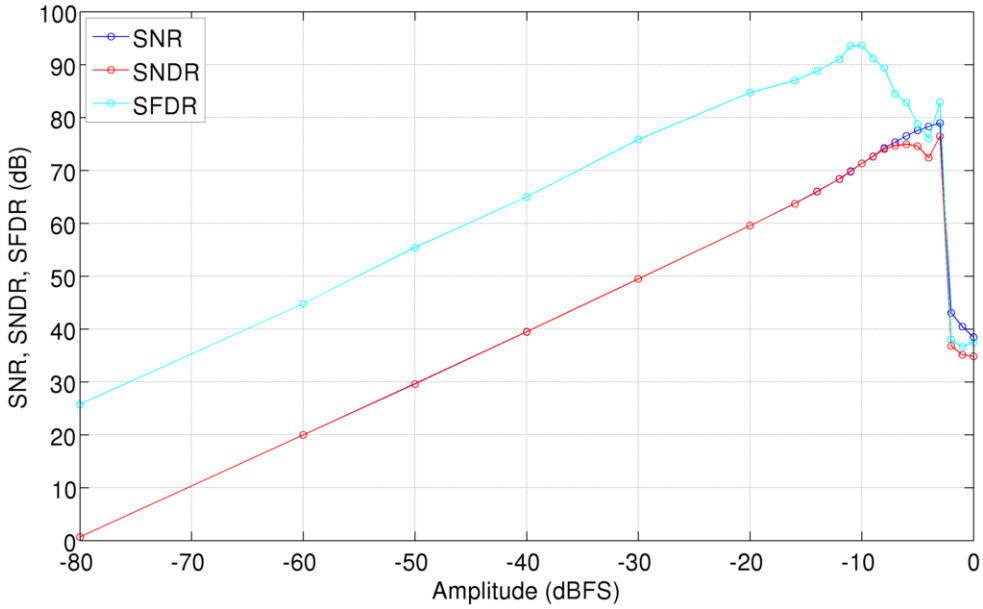


Figure 5.14: ADC performance versus input amplitude.

axis represents the corresponding metric in dB.

As the input amplitude approaches 0 dBFS a large drop-off is observed in the SNR, SNDR and SFDR. The metrics fall from around 80 dB at -4 dBFS to around 40 dB at -3 dBFS. This is normal behavior for a delta-sigma modulator and is the result of the quantizer becoming overloaded, causing the feedback system to become unstable. For a single-bit modulator this typically occurs a few dB below the full-scale range. In the ADC in this design, the maximum stable amplitude is -4 dBFS.

The SNR, which measures the ratio of the signal to the sum of the in-band noise components, is expected to increase monotonically as the input amplitude is increased. This is because the noise floor is constant and the signal harmonics are excluded. This trend is observed in the amplitude sweep and the peak SNR of the ADC is measured to be 78.93 dB.

The SNDR measures the ratio between the signal and the sum of the in-band noise including the harmonic distortion components. It is expected that the SNDR will increase linearly until the harmonics exceed the noise floor, at which point the curve will flatten out and then begin to fall. This expectation is consistent with the

measurement results and the peak SNDR in the amplitude sweep is 76.43 dB. The SNDR is used to determine the effective number of bits (ENOB) of the ADC using Equation 2.26. The measured SNDR corresponds to an effective resolution of 12.40 bits.

The SFDR, which measures the ratio between the signal and the largest spurious tone, is the primary metric used to characterize the linearity of the receiver. Similar to the SNDR, it is expected that in the amplitude sweep the SFDR will increase linearly until the harmonics exceed the noise floor, at which point it will level off and start decreasing. From the amplitude sweep the peak SFDR of the ADC is 93.60 dB.

To further illustrate the maximum SFDR, Figure 5.15 shows the output spectrum of the ADC with a -10 dBFS input signal at 10 kHz. This corresponds to the case where the peak SFDR was achieved in the amplitude sweep in Figure 5.14. Additionally, the plot is zoomed in on the 50 kHz ADC bandwidth to more clearly show the relevant portion of the spectrum. The input signal is clearly visible at 10 kHz with an amplitude of -10 dBFS. The largest spurious signal is the 3rd harmonic with an amplitude of -103.60 dB at approximately 30 kHz. Recall that the input frequency isn't precisely 10 kHz, which is why the 3rd harmonic is seen slightly above 30 kHz.

The SNR, SNDR and SFDR were also tested over the full range of possible frequencies, from 300 Hz to 50 kHz. Figure 5.16 shows the frequency sweep performance. A -10 dBFS input amplitude was used in this test because that was the amplitude which resulted in the maximum SFDR in the amplitude sweep. The ADC performance is consistent over the entire frequency range with the exception of the SFDR, which increases for frequencies above 20 kHz. This is caused by the fact that as the input frequency approaches the upper-end of the range, the harmonics start to move out of the ADC bandwidth. For example, when the input frequency is 30 kHz, the 2nd harmonic is at 60 kHz and the 3rd harmonic is at 90 kHz, both of which are out of band.

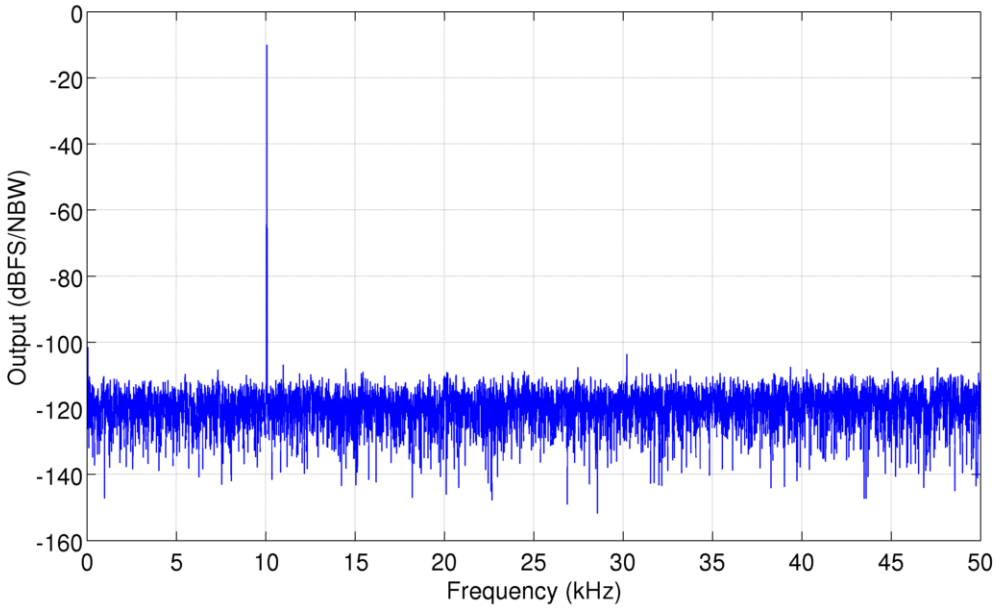


Figure 5.15: ADC output spectrum with the peak SFDR.

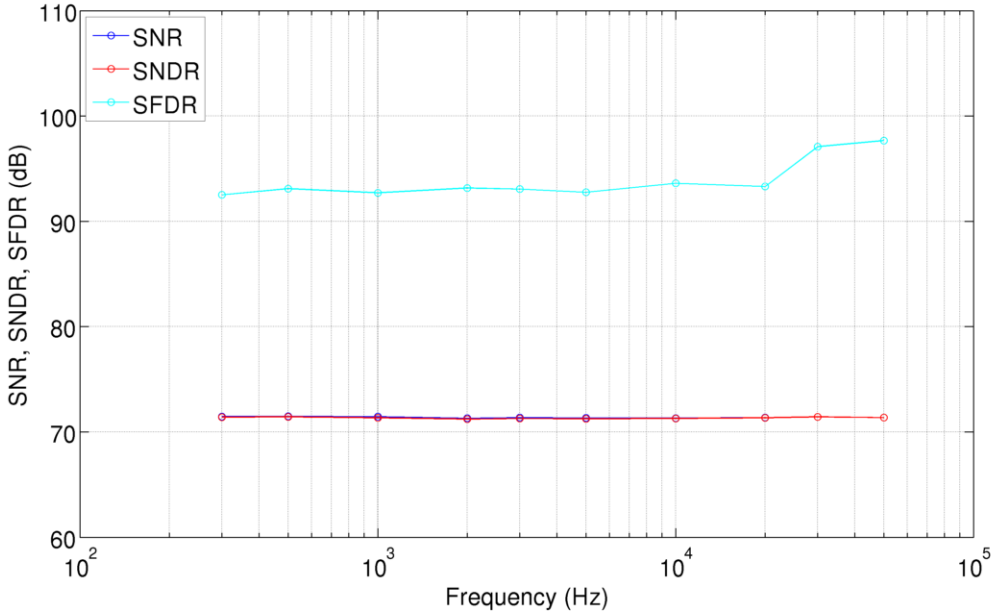


Figure 5.16: ADC performance versus input frequency.

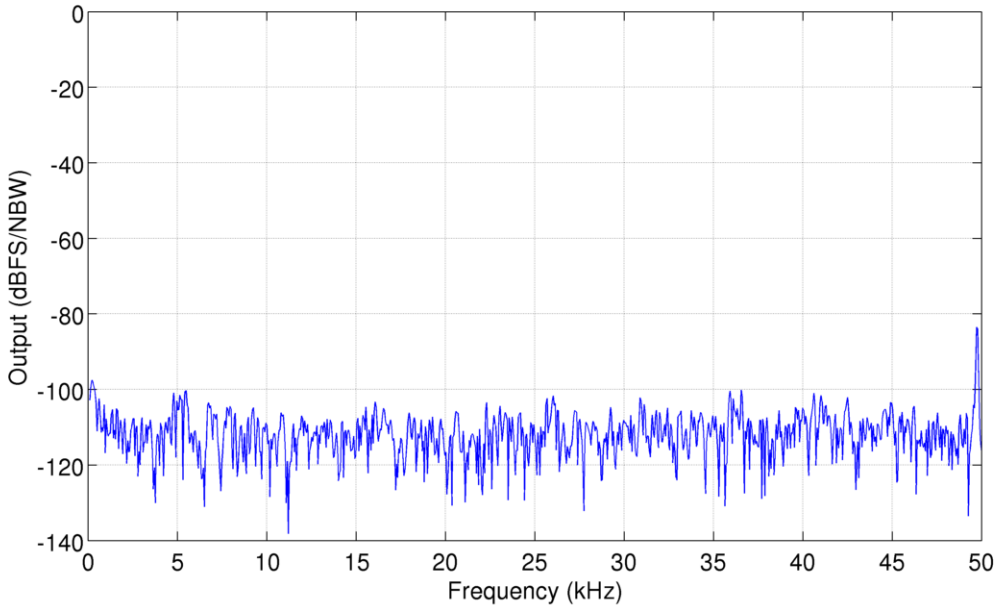


Figure 5.17: ADC output spectrum with a 14.95 MHz input signal.

5.2.4 Anti-Alias Filtering

The implicit anti-alias filter of the continuous-time delta-sigma modulator is measured by inputting a signal with a frequency that is close to the clock frequency, such that it will alias to within the signal band. The aliased signal can then be measured to determine the amount of alias rejection provided by the ADC. The SR-1 signal generator is only capable of producing signals up to 200 kHz, so a different input signal source is needed. For this purpose, a BK Precision 4086 80 MHz Function Generator is used in place of the SR-1. The rest of the ADC test setup remains unchanged.

The input signal is a -20 dBFS sinusoidal signal at 14.95 MHz, which is the worst case frequency for aliasing. It is important to point out that the 4086 function generator is only capable of a single-ended output. The ADC expects a fully-differential signal so the input signal is adjusted accordingly. Figure 5.17 shows the in-band output spectrum from the aliasing test.

The 14.95 MHz signal aliases to approximately 50 kHz and is visible at the far

Table 5.2: ADC measurement results summary.

Measurement	Value
Peak SNR (dB)	78.93
Peak SNDR (dB)	76.43
Peak SFDR (dB)	93.60
ENOB (bits)	12.40
Alias Rejection (dB)	63.63
Power Dissipation (µW)	641.52

right of the spectrum. The strength of the signal is −83.63 dBFS, which corresponds to an alias rejection of 63.63 dB from the −20 dBFS input signal. It is important to note that this test is the worst case aliasing. Any other frequency will either see more alias rejection, or will alias to a frequency that is out of band. In addition to the alias tone, it would appear that there are several other small spurious signals visible in the output spectrum. This is likely caused by the single-ended input signal used in this test, which is more susceptible to interference.

5.2.5 Summary

The ADC was characterized in terms of its dynamic performance. The peak SNR was 78.93 dB. The peak SNDR was 76.43 dB, which corresponds to an effective resolution of 12.40 bits. The ADC linearity was measured in terms of its peak SFDR, which was 93.60 dB. The implicit anti-alias filter was measured to have a worst-case alias rejection of 63.63 dB. Finally, the power dissipation of the ADC was 641.52 µW, which was measured using a BK Precision 5492 5 1/2 Digit Multimeter.

Table 5.2 shows a summary of the ADC measurement results. The peak SNR, peak SNDR and peak SFDR values are all derived from the amplitude sweep, which was performed with an input frequency of 10 kHz. The alias rejection measurement was performed with a 14.95 MHz input signal.

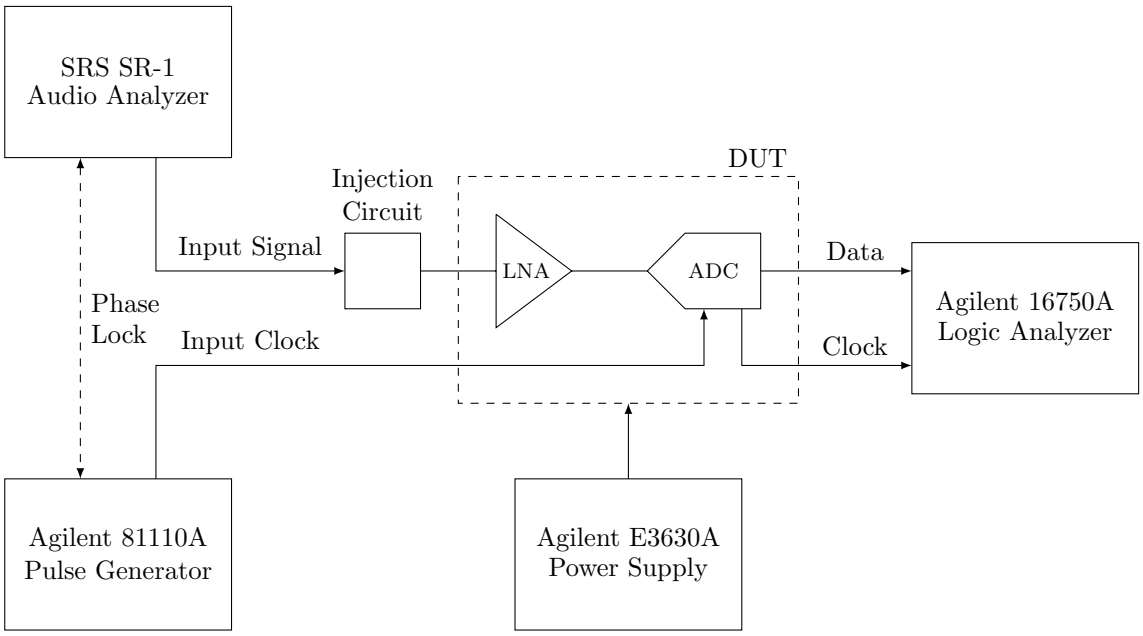


Figure 5.18: Test setup for receiver measurements.

5.3 Receiver Measurement Results

5.3.1 Test Setup

The test setup for the receiver measurements is shown in Figure 5.18. The setup is very similar to the ADC test setup. The input signal is generated by the Stanford Research System SR-1 Audio Analyzer, which is used for its good distortion performance that doesn't require any additional filtering of the input signal. The SR-1 outputs a fully-differential signal and is connected to the injection circuit with a shielded XLR cable. The injection circuit consists of a passive voltage to current converter, a dummy 1 Ω, 1 mH antenna and an input transformer. The fully-differential output of the LNA is fed directly to the input of the ADC.

The clock signal for the ADC is generated by the Agilent 81110A Pulse Generator. This clock source was selected for its good jitter performance. The 81110A is configured to output a single-ended 1.2 V square wave at 15 MHz. In addition to connecting the clock signal to the ADC, it is also connected to the external reference port on the SR-1 to facilitate phase-locking between the signal source and the clock

source. This is done to prevent spectral smearing in the output spectrum.

The receiver output is captured by an Agilent 16750A Logic Analyzer. The single-chip receiver outputs two digital signals. The first is the 1-bit data stream. The second is the corresponding 15 MHz clock. The logic analyzer is operated in state mode, which means that it captures data synchronously with the 15 MHz clock from the receiver. The data is saved to files on the logic analyzer and then transferred to a PC for analysis in MATLAB.

The receiver is powered by an Agilent E3630A DC Power Supply. The power supply is configured to output 1.2 V. Separate power and ground connections are used for each portion of the receiver to prevent noise coupling. There are five separate power connections: LNA analog supply, ADC analog supply, ADC digital supply, ADC reference voltage and ESD protection supply. Each power connection has its own dedicated decoupling network.

5.3.2 Dynamic Performance

The full receiver can be characterized using the same dynamic performance metrics as the ADC, which are the SNR, SNDR and SFDR. The peak values of these three metrics are determined by sweeping the amplitude of the input signal and analyzing the digital signal at the output of the receiver. A separate sweep is performed for each LNA gain mode. The receiver amplitude sweeps for each gain mode are shown in Figures 5.19 to 5.22. In some cases, particularly in mode 0, the SNR and SNDR are difficult to differentiate because they are equal over much of the amplitude sweep. A 10.070801 kHz input frequency was used and the amplitude was swept from -18 dBFS to -3 dBFS. The value of the amplitude corresponds to the amplitude of the signal at the input of the ADC, which is not the same as the amplitude at the input of the LNA. By specifying the amplitude in this way the results are consistent with the ADC results shown in the previous section. The receiver output data was analyzed in MATLAB using a 2,097,152 point FFT with a Hann window.

The peak SNR is different in each gain mode. The peak SNR in mode 0, mode 1, mode 2 and mode 3 are 58.31 dB, 66.71 dB, 74.29 dB and 77.98 dB respectively.

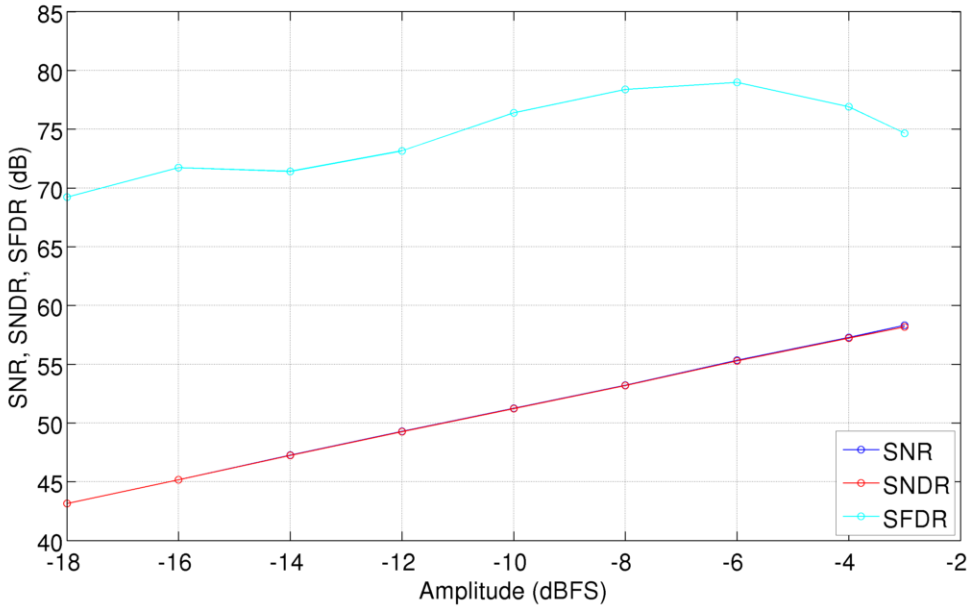


Figure 5.19: Receiver performance versus input amplitude in mode 0.

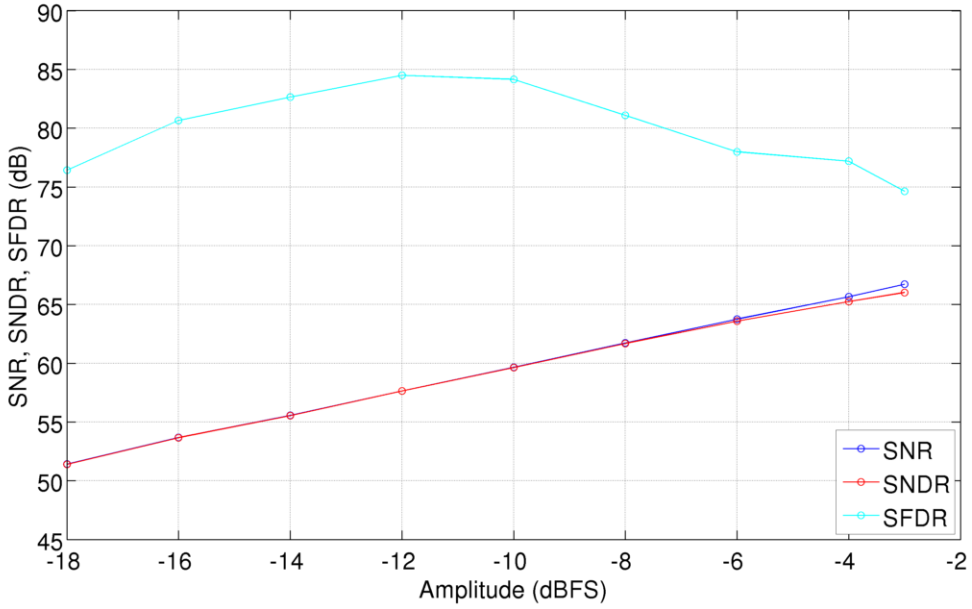


Figure 5.20: Receiver performance versus input amplitude in mode 1.

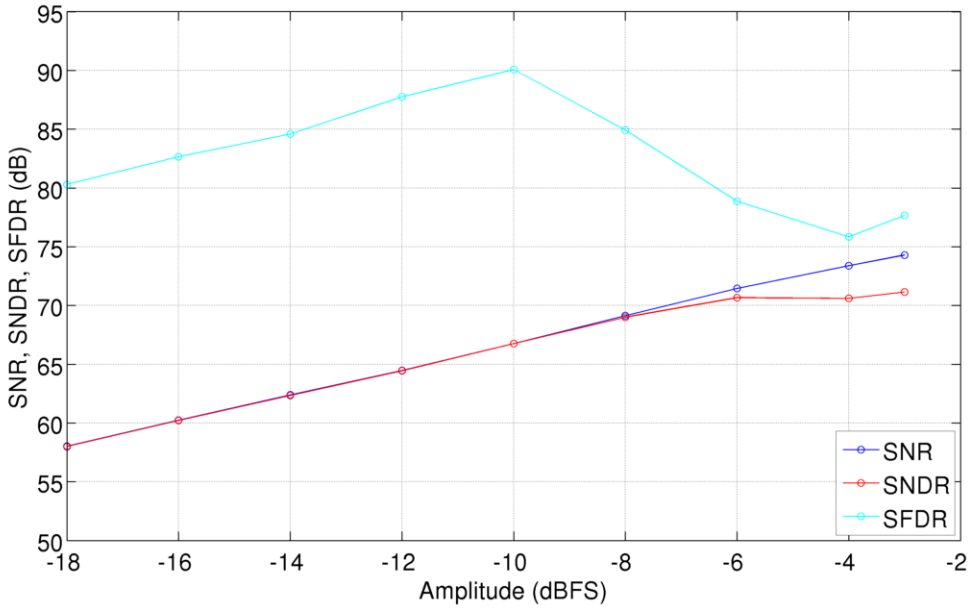


Figure 5.21: Receiver performance versus input amplitude in mode 2.

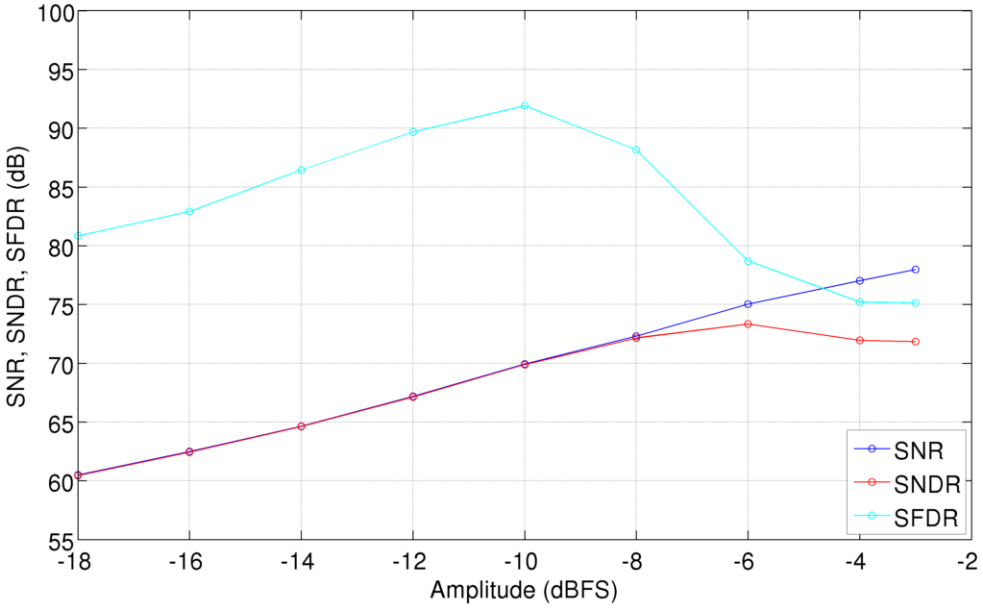


Figure 5.22: Receiver performance versus input amplitude in mode 3.

The change in signal-to-noise ratio is due to the fact that the noise from the LNA sets the noise floor of the output spectrum in all but the lowest gain mode. As shown in Figure 5.4, the noise floor at the output of the LNA roughly scales with the gain. Only in mode 3, the lowest gain mode, is the noise floor slightly below the noise floor of the ADC. The SNDR follows a similar trend as the SNR except when the signal amplitude becomes large, in which case the distortion terms cause it to level off. The peak SNDR in mode 0, mode 1, mode 2 and mode 3 are 58.19 dB, 66.02 dB, 71.14 dB and 73.33 dB respectively.

The SFDR also varies in the different LNA gain modes. The peak SFDR in mode 0, mode 1, mode 2 and mode 3 are 78.98 dB, 84.50 dB, 90.08 dB and 91.91 dB respectively. The amplitude where the peak SFDR occurs is also different in each more. In the higher gain modes, mode 0 and mode 1, the peak occurs at -6 dBFS and -12 dBFS. In contrast, in the lower gain modes, mode 2 and mode 3, the peak occurs at -10 dBFS in both cases. This difference is likely due to the fact that the LNA limits the SFDR in the higher gain modes, while the ADC limits in the SFDR in the lower gain modes. Recall that the peak SFDR of the ADC also occurred at -10 dBFS.

To further illustrate the linearity of the receiver, the output spectrum is shown for each gain mode with the input amplitude that produced the peak SFDR. Figures 5.23 to 5.26 show the output spectrum of the receiver in each gain mode. There are two features to point out in these figures. First, the spurious tones at the far left of the spectrum are due to the 60 Hz power line noise that was first encountered when measuring the LNA. Second, notice that the noise floor decreases as the gain is reduced, which agrees with peak SNR trend discussed above.

In addition to performing the amplitude sweep, it is also important to sweep the frequency range to uncover any frequency dependent effects in the receiver. To accomplish this, the amplitude of the input signal is set to the value that resulted in the maximum SFDR in the amplitude sweep, then the frequency is swept from 300 Hz to 50 kHz. A separate frequency sweep is performed for each LNA gain mode. Figures 5.27 to 5.30 show the frequency sweeps for each gain mode.

The SNR and SNDR both have consistent performance over the entire frequency

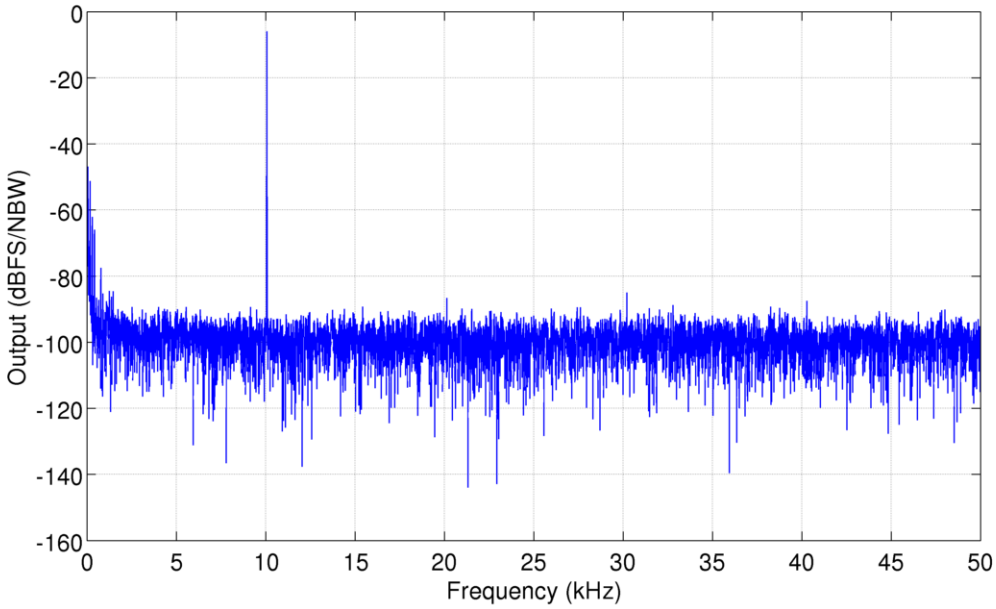


Figure 5.23: Receiver output spectrum with the peak SFDR in mode 0.

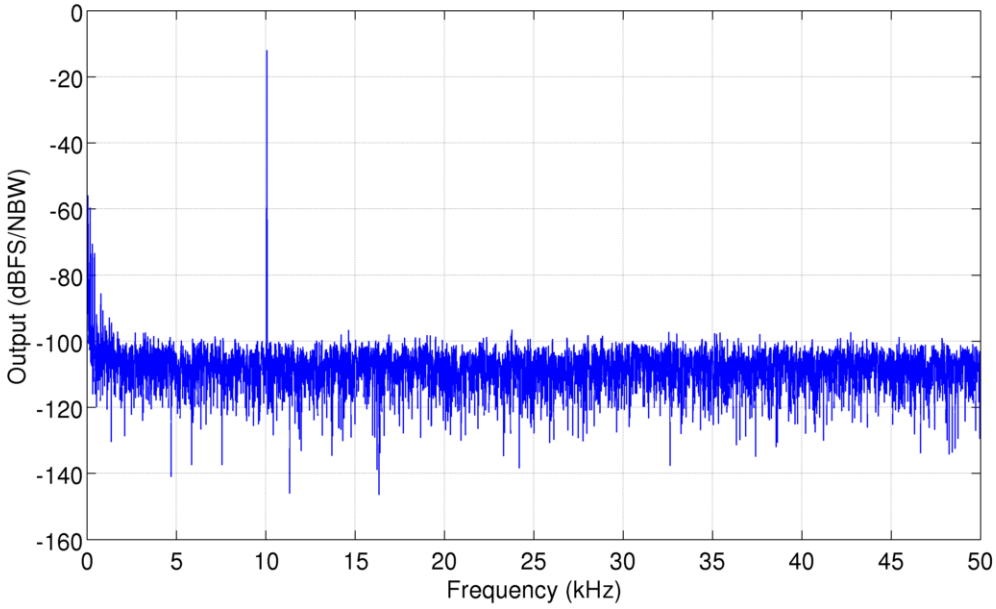


Figure 5.24: Receiver output spectrum with the peak SFDR in mode 1.

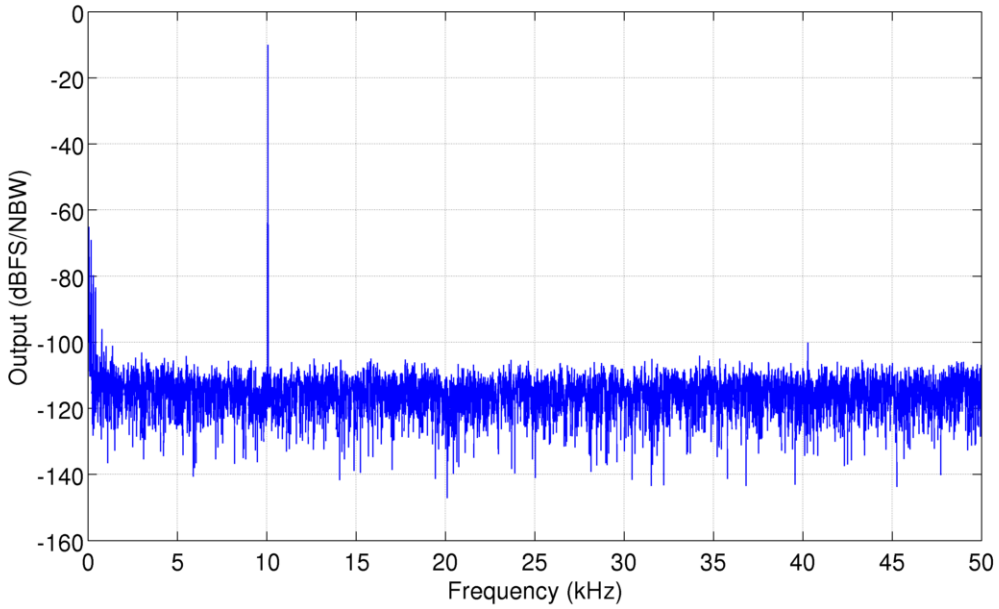


Figure 5.25: Receiver output spectrum with the peak SFDR in mode 2.

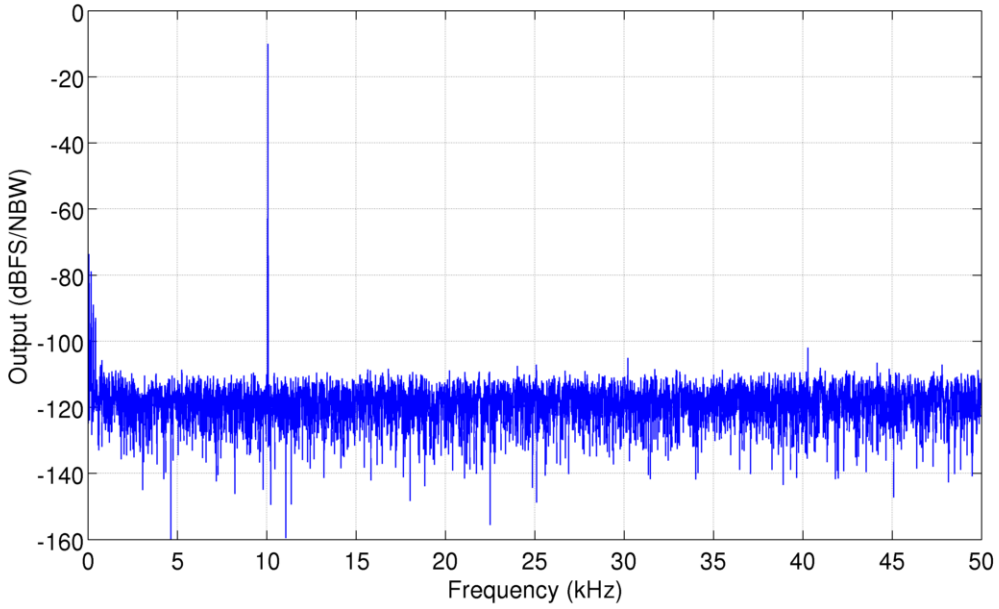


Figure 5.26: Receiver output spectrum with the peak SFDR in mode 3.

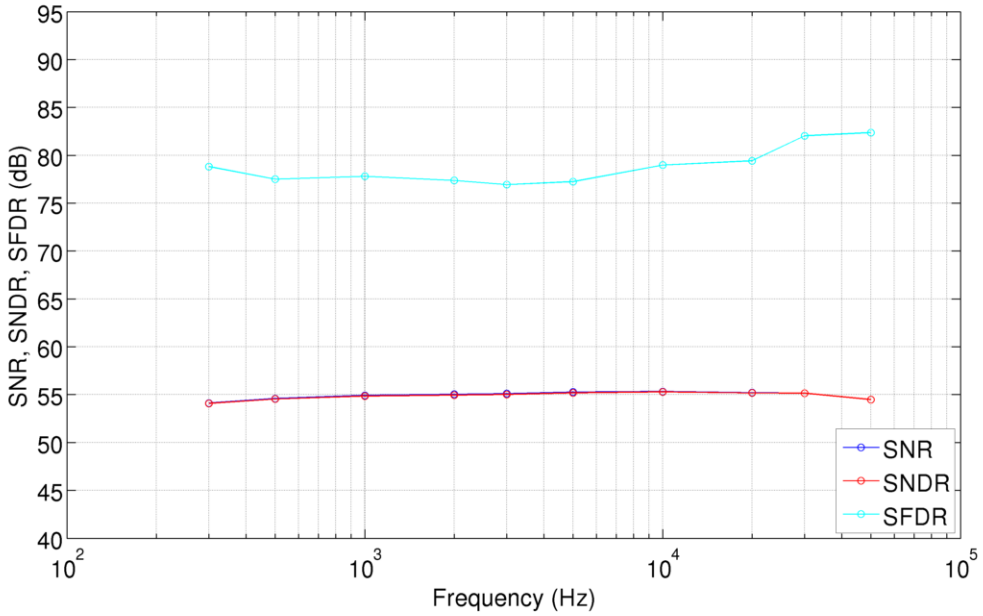


Figure 5.27: Receiver performance versus input frequency in mode 0.

range in all of the gain modes. There is a slight decrease in the SNR and SNDR at 300 Hz, but this can be attributed to the roll-off of the LNA gain at low frequencies. The SFDR also maintains approximately equivalent performance over the frequency sweeps, which confirms the peak SFDR results measured in the amplitude sweeps. There is a small increase in the SFDR at the highest test frequencies (30 kHz and 50 kHz). This increase is the result of the harmonics falling outside the receiver bandwidth. Interestingly, this increase is visible in all of the gain modes except mode 1. In this mode the input amplitude is the smallest of any test case (-12 dBFS) and the SFDR is determined by the noise floor, not the largest harmonic, which explains why there is no jump in the SFDR at the highest input frequencies.

5.3.3 Noise Coupling

The noise coupling between the ADC and LNA can be characterized by measuring the output spectrum of the LNA with the ADC off and comparing it with a measurement of the LNA output spectrum with the ADC on. By doing this, any noise that couples

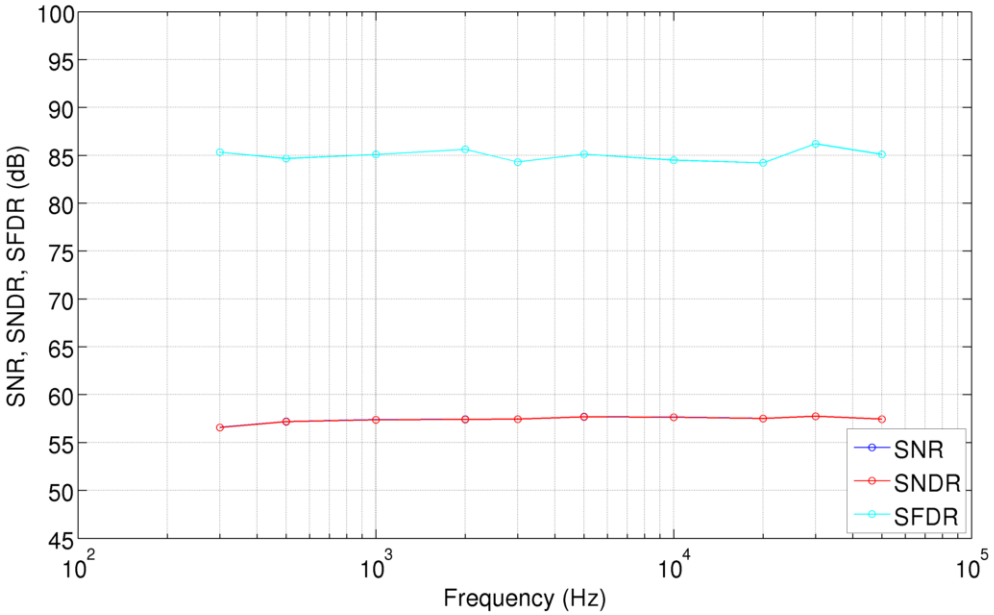


Figure 5.28: Receiver performance versus input frequency in mode 1.

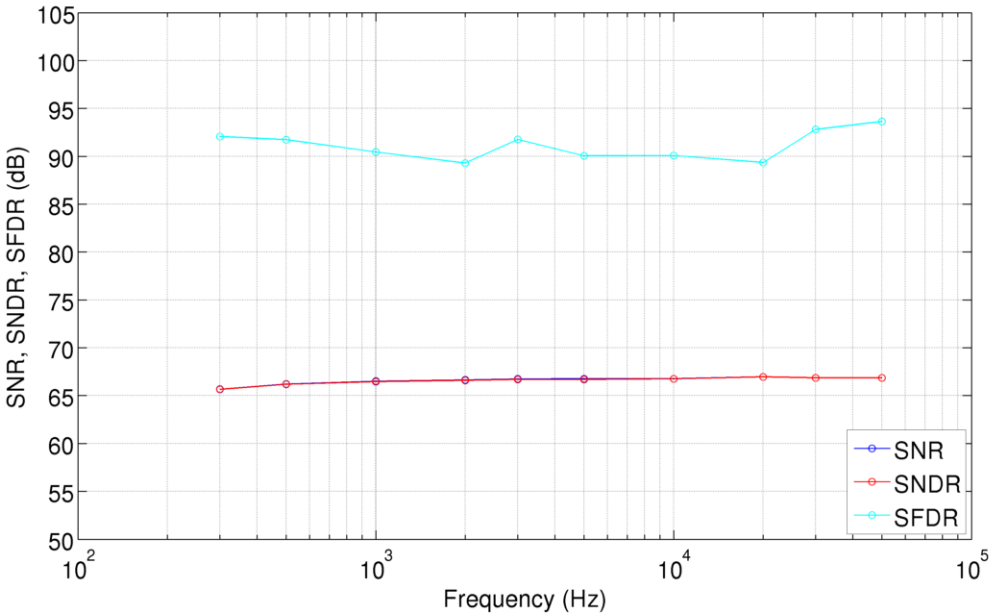


Figure 5.29: Receiver performance versus input frequency in mode 2.

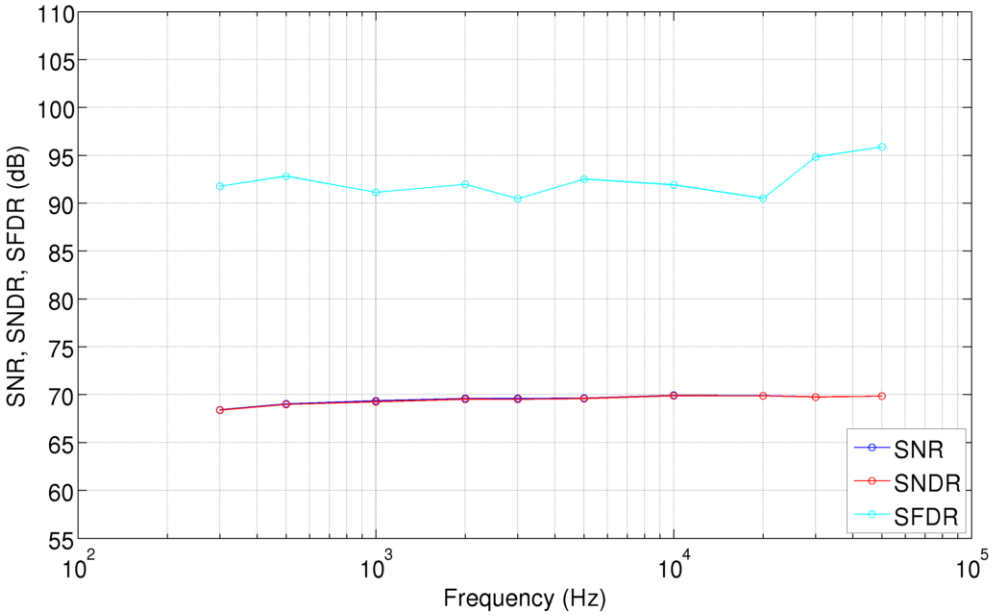


Figure 5.30: Receiver performance versus input frequency in mode 3.

from the ADC can be differentiated from the normal LNA output spectrum. To ensure a realistic comparison, when the ADC is on it is connected such that it is also processing the output signal of the LNA, rather than sitting idle. A 10 kHz input signal is used for the comparison and the measurements are repeated for each LNA gain mode. A larger -6 dBFS input amplitude is used in this test to ensure that the distortion terms are visible in the output spectrum. Figures 5.31 to 5.34 show the noise coupling comparison for each gain mode. In each of the figures, the top spectrum is with the ADC off and the bottom spectrum is with the ADC on.

Given the proximity of the LNA and the ADC on the die, noise coupling could be a serious issue that could significantly degrade the performance of the receiver. However, the LNA output spectrum comparisons show only minor differences when the ADC is off versus when the ADC is on. In all of the gain modes, the noise floor is unchanged when the ADC is turned on. Further, the amplitude of the 10 kHz input tone is the same and the amount of power line noise (60 Hz and its harmonics) is the same. The only noticeable difference is the amplitude of the distortion terms. The worst case is mode 0, where the 3rd harmonic (30 kHz) increases slightly causing a

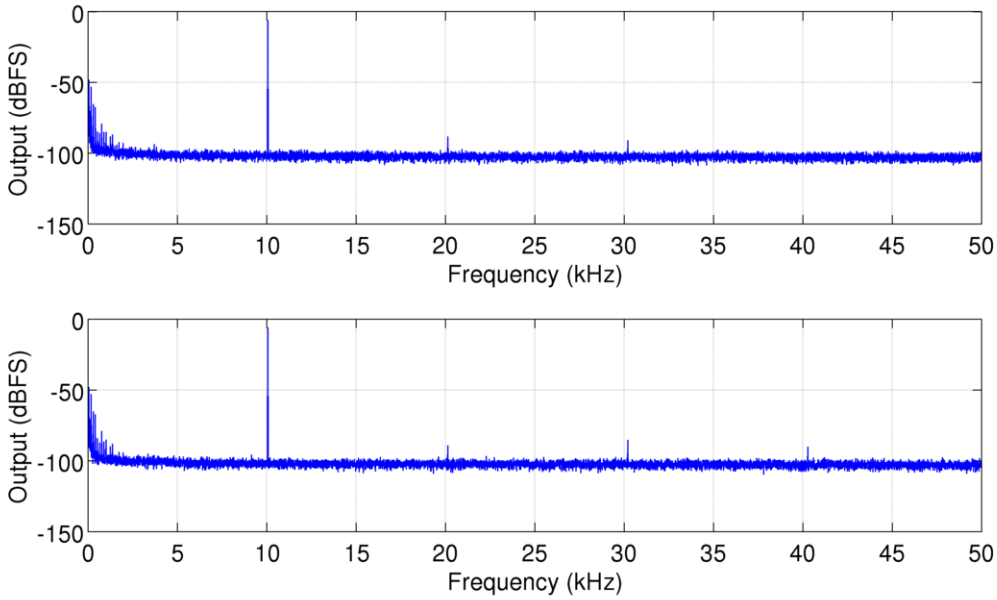


Figure 5.31: LNA output spectrum with ADC off (top) and on (bottom) in mode 0.

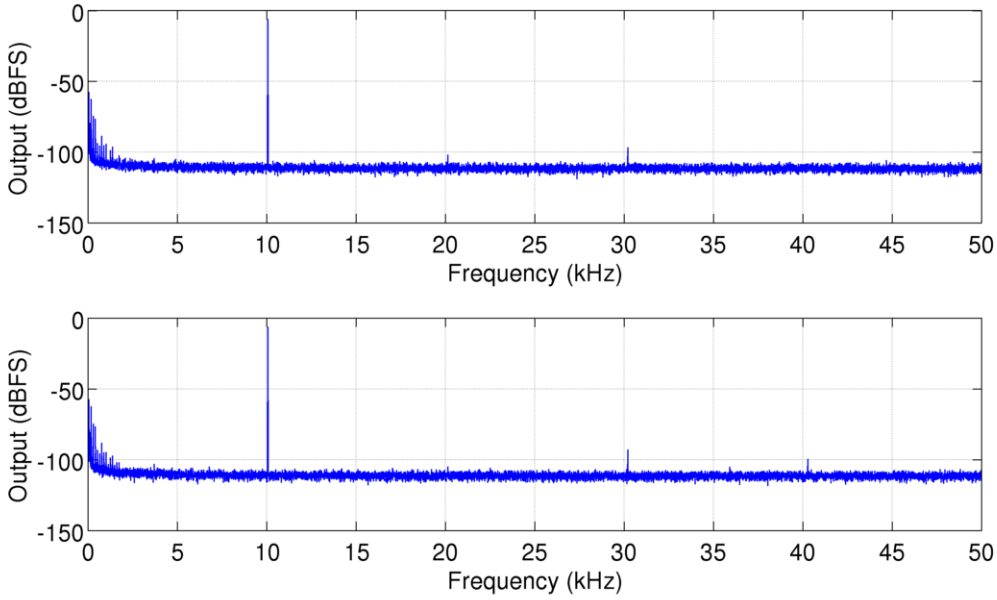


Figure 5.32: LNA output spectrum with ADC off (top) and on (bottom) in mode 1.

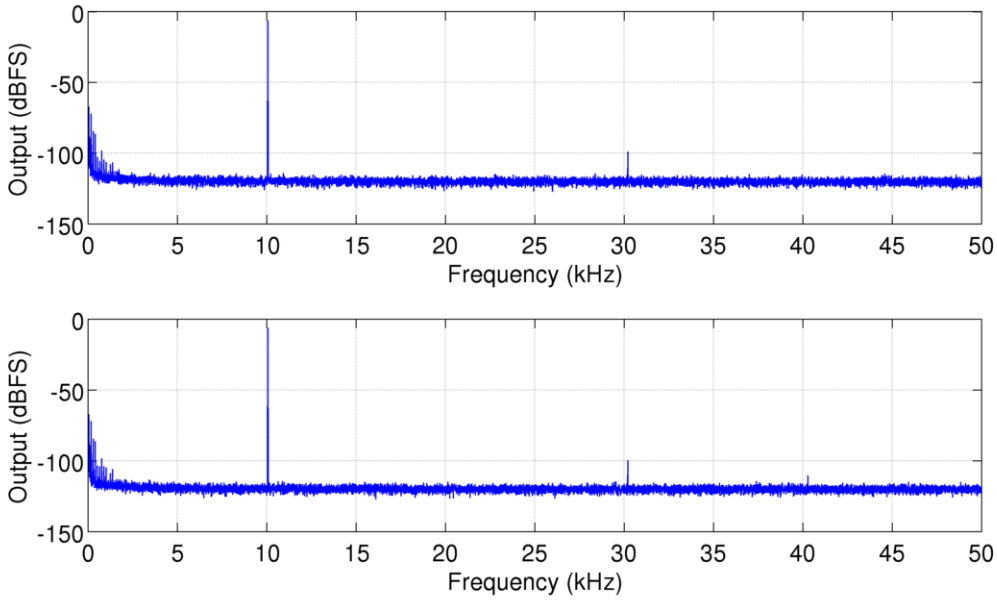


Figure 5.33: LNA output spectrum with ADC off (top) and on (bottom) in mode 2.

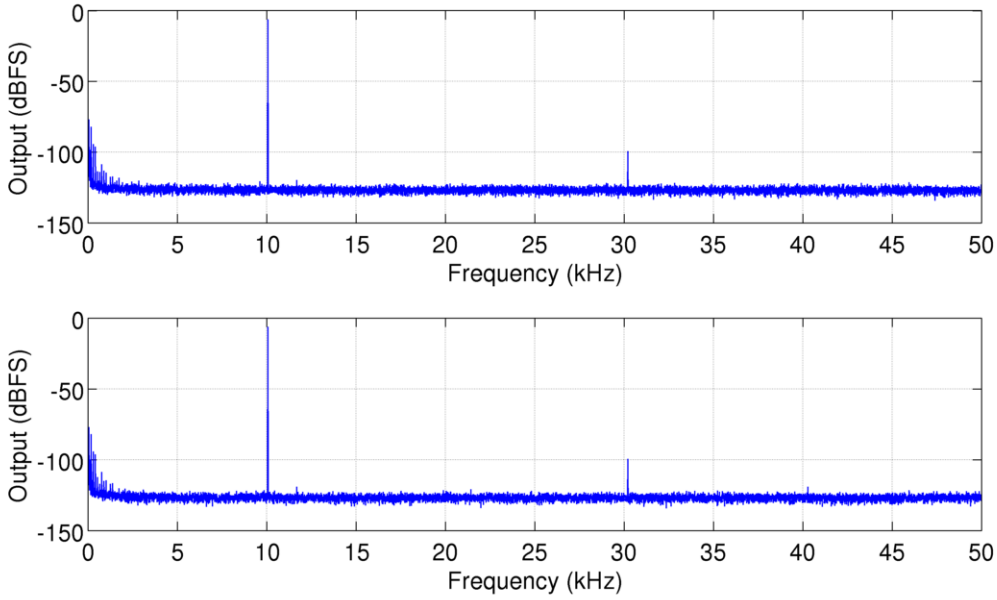


Figure 5.34: LNA output spectrum with ADC off (top) and on (bottom) in mode 3.

reduction of the SFDR by approximately 3 dB. This reduction in SFDR is only visible in the two highest gain modes. In the two lower gain modes the SFDR is unchanged. It is likely that the higher gain modes have slightly reduced performance due to the fact that any coupled noise is amplified by a larger amount. Overall these results validate the precautions taken to reduce noise coupling between the noisy ADC and the sensitive LNA, as only minor differences in the output spectrum are visible.

5.3.4 Anti-Alias Filtering

The anti-alias filtering performance of the receiver is determined by inputting a signal at a frequency that will alias to within the signal band and then measuring the strength of the aliased signal. The worst-case aliasing occurs when an interfering signal is 50 kHz below the clock rate of 15 MHz, which is 14.95 MHz. The SR-1 signal generator is not capable of generating signals above 200 kHz, so a BK Precision 4086 80 MHz Function Generator is used in its place. The rest of the receiver test setup is unchanged. For this test a 0 dBFS single-ended sinusoidal signal at 14.95 MHz is connected to the input of the receiver. Figures 5.35 to 5.38 show the output spectrum of the receiver in each gain mode.

The 14.95 MHz input signal aliases to approximately 50 kHz at the output of the receiver. The aliased signal is visible in each output spectrum, although it is difficult to see in mode 0 due to the higher noise floor. In mode 1, for example, the aliased signal has an amplitude of -82.69 dBFS. With an input amplitude of 0 dBFS, this corresponds to an alias rejection of 82.69 dB. The alias rejection in mode 0, mode 1, mode 2 and mode 3 are 82.34 dB, 82.69 dB, 84.47 dB and 86.61 dB respectively.

The alias rejection of the ADC was measured to be 63.63 dB. This means that the alias rejection of the full receiver is approximately 20 dB higher. This additional rejection can be attributed to the frequency response of the LNA, which rolls off at high frequencies, and to the parasitics of the input transformer. It should also be pointed out that because the 4086 function generator outputs a single-ended signal, additional noise can couple into the input of the receiver and is likely the cause of the small spurious tones and additional noise seen in some of the output spectra.

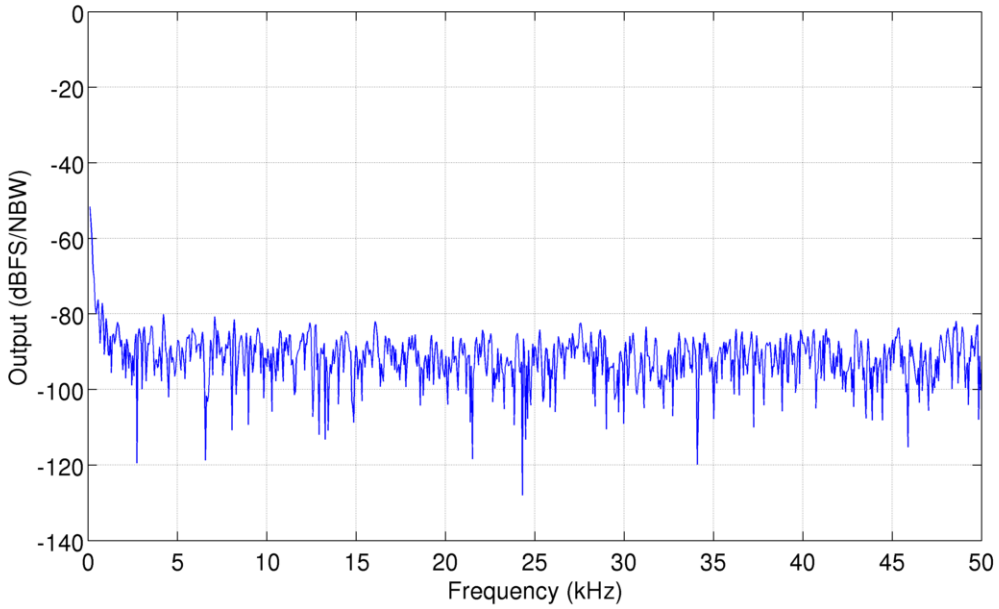


Figure 5.35: Receiver output spectrum with a 14.95 MHz input signal in mode 0.

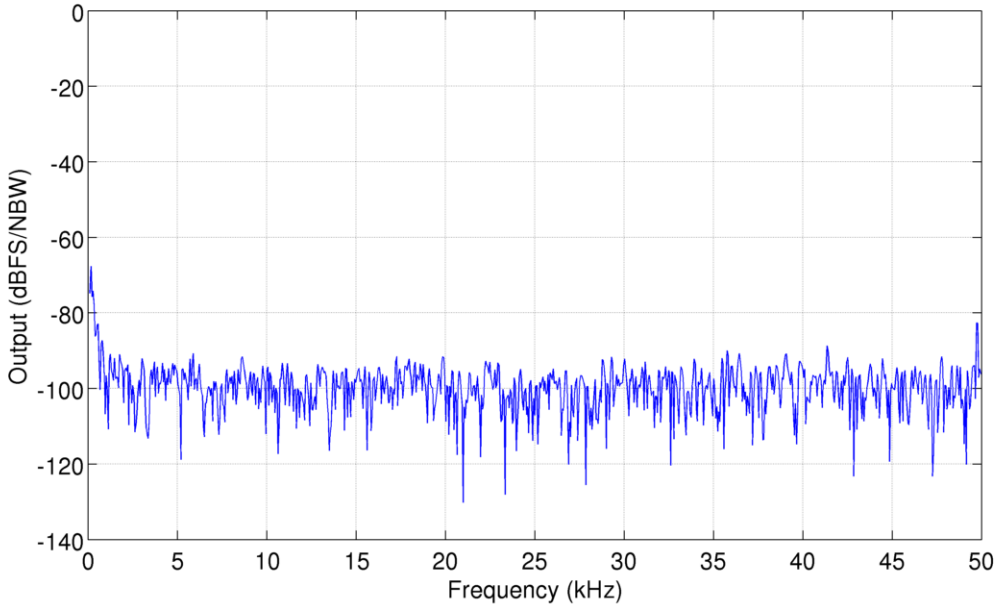


Figure 5.36: Receiver output spectrum with a 14.95 MHz input signal in mode 1.

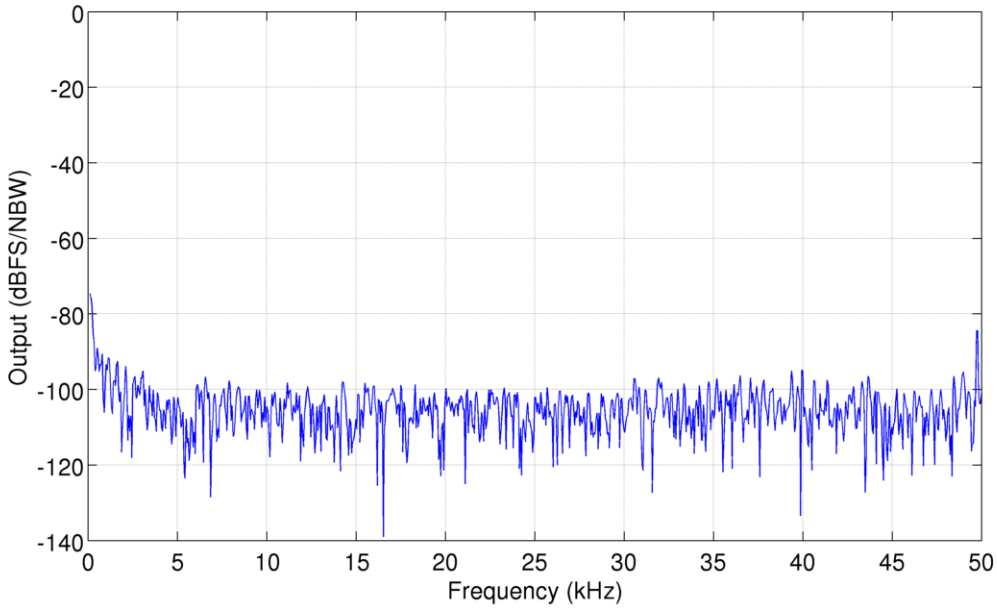


Figure 5.37: Receiver output spectrum with a 14.95 MHz input signal in mode 2.

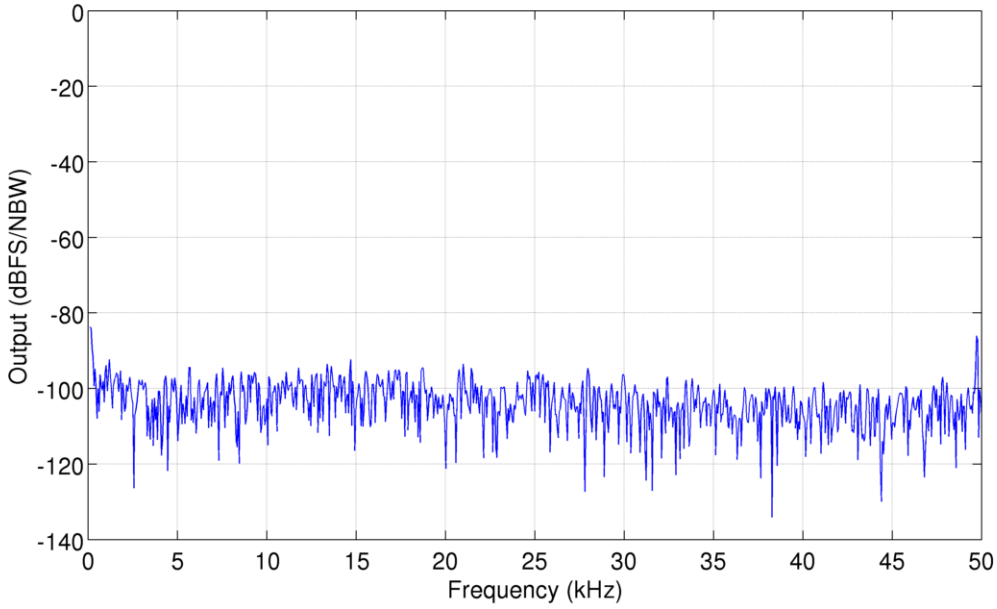


Figure 5.38: Receiver output spectrum with a 14.95 MHz input signal in mode 3.

Table 5.3: Receiver measurement results summary.

Measurement	Mode 0	Mode 1	Mode 2	Mode 3
Peak SNR (dB)	58.31	66.71	74.29	77.98
Peak SNDR (dB)	58.19	66.02	71.14	73.33
Peak SFDR (dB)	78.98	84.50	90.08	91.91
Alias Rejection (dB)	82.34	82.69	84.47	86.61
Power Dissipation (mW)	1.5494	1.5512	1.5506	1.5516

5.3.5 Summary

The receiver was characterized in terms of the same dynamic performance metrics that were used to characterize the ADC (SNR, SNDR, SDFR). The receiver performance was different in each gain mode, with the peak SNR varying from 58.31 dB to 77.98 dB. The peak SNDR varied over a range of 58.19 dB to 73.33 dB. The peak SFDR varied from 78.98 dB to 91.91 dB. The anti-alias filtering capability of the receiver exceeded the 80 dB design goal, with values ranging from 82.34 dB to 86.61 dB. The power dissipation of the full receiver was approximately 1.55 mW in all of the gain modes, which is roughly equivalent to the sum of the LNA power dissipation and the ADC power dissipation. The power dissipation was measured with a BK Precision 5492 5 1/2 Digit Multimeter.

Table 5.3 shows a summary of the receiver measurement results. The peak SNR, peak SNDR and peak SFDR values were all derived from the amplitude sweeps, which were performed with an input frequency of 10 kHz. The alias rejection measurement used a 14.95 MHz test signal.

5.4 Field Test Results

5.4.1 Test Setup

The test setup used for field measurements is shown in Figure 5.39. The input signal was generated by a loop antenna already installed at the test sites. The antenna was connected directly to the input transformer. The passive voltage to current converter

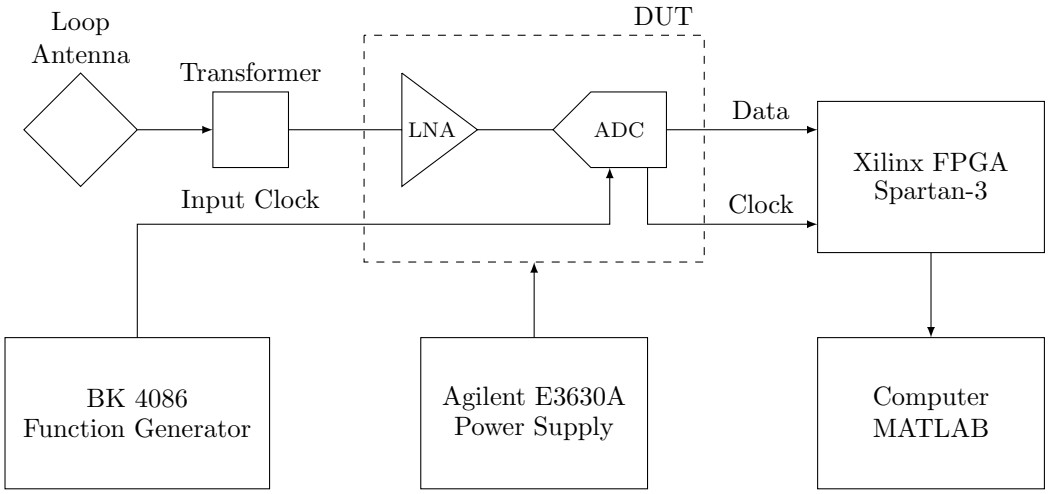


Figure 5.39: Test setup for field measurements.

and the dummy antenna are not used for field measurements. While the VLF loop antennas vary in size and shape, they all have a 1 Ω, 1 mH impedance, which is connected to the input of the LNA with the 24:548 center-tapped transformer. The output of the LNA is fed directly to the input of the ADC.

The clock signal for the ADC was generated with a BK Precision 4086 80 MHz Function Generator. The 4086 has slightly worse jitter performance than the Agilent 81110A Pulse Generator used in the lab measurements. However, it was tested in the lab and did not noticeably degrade the performance of the ADC. The clock source was configured to generate a 1.2 V square wave at 15 MHz. The 4086 was selected for the field test measurements due to its smaller size and weight when compared to the 81110A.

The receiver was powered by an Agilent E3630A DC Power Supply, which was configured to output 1.2 V. Separate power and ground connections were made to the test board to prevent noise coupling between the various parts of the test chip. There were five separate power connections: LNA analog supply, ADC analog supply, ADC digital supply, ADC reference voltage and ESD protection supply. Each of the connections had its own dedicated decoupling network on the test board.

The digital output data from the receiver was captured by a FPGA and streamed

to a laptop computer in real-time to monitor the received signal. A TXB0104 level-shifter (not shown) was placed between the test board and the FPGA to convert the 1.2 V digital output data from the receiver to 3.3 V digital data, which is expected by the FPGA input pins. The level-shifter also provided an extra layer of isolation between the receiver and the FPGA to prevent any coupling of noise between the two systems.

A Xilinx Spartan-3 XC3S1500 FPGA was used in this application. The FPGA was programmed to collect the two input signals from the receiver: the 1-bit data stream and the 15 MHz clock. The clock signal from the chip was used to synchronously capture the receiver output data on the FGPA. The data was then buffered in the FPGA's onboard RAM and streamed over USB in real-time to a nearby laptop. Finally, the data was processed in MATLAB to produce a spectrogram of the received signal.

5.4.2 Stanford Field Test

The first field test was performed at Stanford University on the roof of the Packard Electrical Engineering building. This test used an existing loop antenna that was installed by the Stanford VLF research group. This antenna consists of two perpendicular loops. One loop faces in the north-south direction and the other faces in the east-west direction. The north-south loop was used in this experiment. Each loop is a square that is roughly 2 meters on each side with 11 turns of wire. Given that this test site is in an urban environment with many nearby sources of interference, it was expected that the output data would be very noisy. As a result, the lowest gain mode of the receiver was used to prevent the output from saturating.

Figure 5.40 shows 60 seconds of data collected using the north-south antenna and the lowest gain mode. The spectrogram shows how the spectral content of the received signal changes over time. The horizontal axis represents time, the vertical axis represents frequency and the color represents the strength of the signal.

The horizontal lines in the spectrogram are VLF transmitters that output at a constant frequency. The two strongest transmitters in this spectrogram are at 24.8

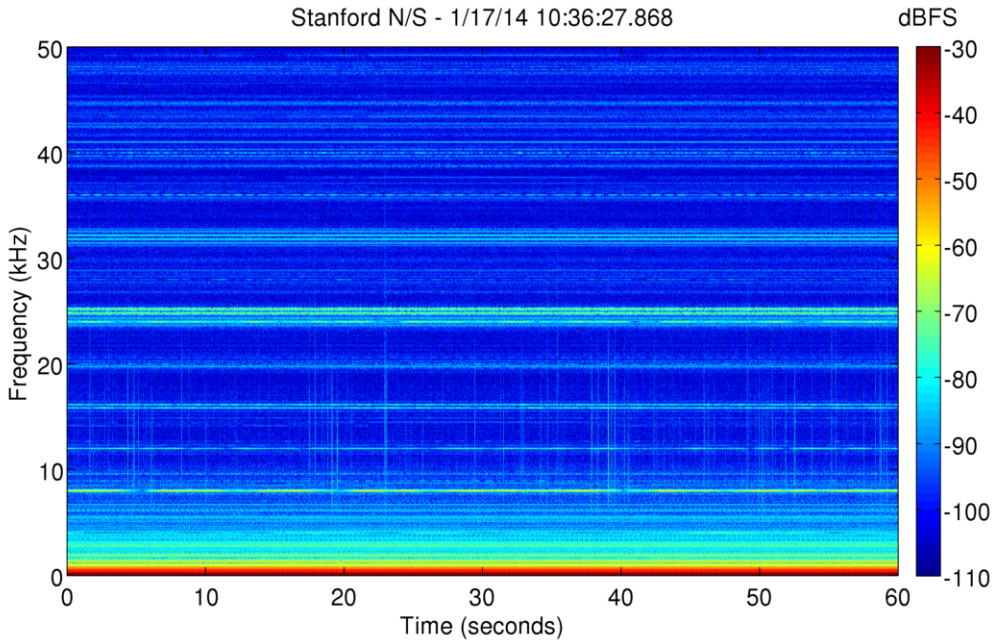


Figure 5.40: Spectrogram showing 60 seconds of data collected at Stanford University.

kHz and 25.2 kHz. These are the NLK transmitter in Jim Creek, Washington (24.8 kHz) and the NML transmitter in LaMoure, North Dakota (25.2 kHz) [18]. These transmitters are used by the US Navy for communication with submerged submarines.

The vertical lines in the spectrogram that extend from roughly 5 kHz to 20 kHz are radio atmospherics, or sferics for short. These are impulsive signals generated by lightning strikes, which can propagate thousands of kilometers from their source in the Earth-ionosphere waveguide.

There is also a large amount of interference visible in the spectrogram, particularly at frequencies below 5 kHz. In fact, the strongest frequency component in the received signal is the 60 Hz power line noise. This amount of interference is expected given the urban environment where the antenna was installed.

5.4.3 Santa Cruz Field Test

The second field test was performed at a site operated by Lockheed Martin in the Santa Cruz Mountains near Santa Cruz, California. The test site is in a remote area,

far away from any cities, and the antenna is installed over 500 feet from the nearest building. Under these conditions it is expected that there will be much less noise and interference, which will result in a much cleaner received signal. The antenna at this site is a right isosceles triangle with a base of approximately 10 meters and a height of approximately 5 meters. The antenna has 5 turns of wire. This is one of the largest and most sensitive antennas deployed by the Stanford VLF research group. This antenna has two separate loops, one in the north-south direction and one in the east-west direction. The east-west loop was used in this experiment.

Figure 5.41 shows 60 seconds of data collected at the Santa Cruz test site. The LNA gain was set to the lowest gain mode in order to facilitate a direct comparison with the Stanford field test data. There are several noticeable differences between the data collected at Stanford and the data collected at the Santa Cruz site. As expected, there is far less interference visible in the spectrogram and the power line noise below 5 kHz is significantly reduced. There is also an increase in the number of sferics visible in the data, which is due to the better noise environment and the increased sensitivity of the larger antenna.

Many of the same VLF transmitters are visible in the Santa Cruz spectrogram, including the NLK transmitter in Washington at 24.8 kHz and the NML transmitter in North Dakota at 25.2 kHz. One new feature that was not seen in the Stanford data is the set of horizontal dashed lines occurring between 11 kHz and 15 kHz. These pulsating signals are generated by the Russian Alpha navigation system, which is used to determine the position of ships and airplanes. It is likely that these Russian signals are only seen in the data at the Santa Cruz test site due to the east-west orientation of the antenna and the better sensitivity of the large antenna.

5.4.4 Receiver Comparison

The primary receiver currently used by the Stanford VLF research group is the AWESOME receiver. The AWESOME receiver is deployed around the world and is the gold-standard for VLF receiver systems with the highest data quality. An AWESOME receiver was available at the Stanford field test site so a direct comparison

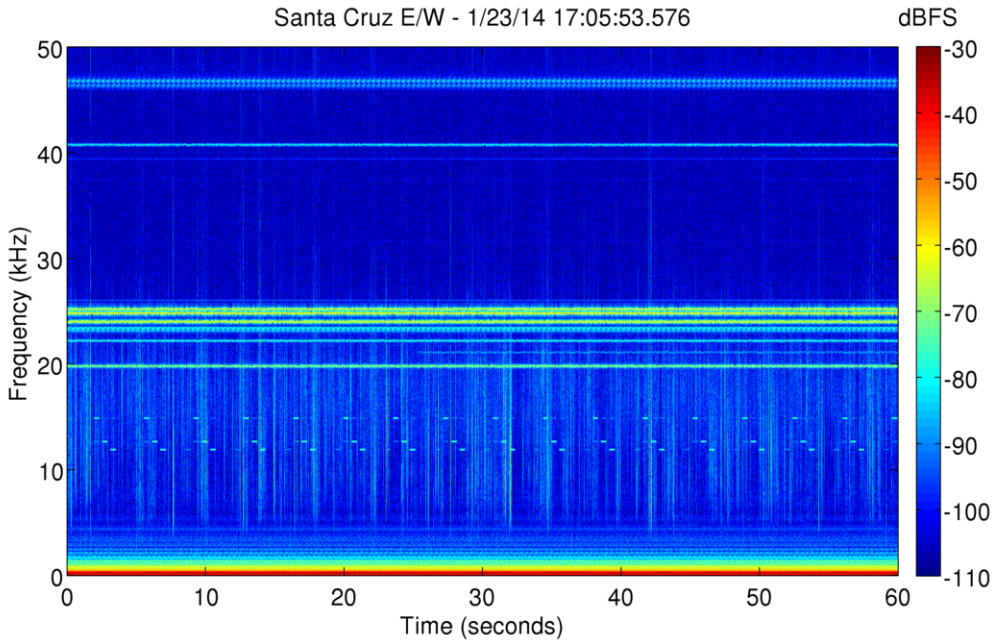


Figure 5.41: Spectrogram showing 60 seconds of data collected in the Santa Cruz Mountains.

can be made between the performance of the single-chip receiver and the AWESOME receiver.

Figure 5.42 shows a side-by-side spectrogram of data received with the AWESOME receiver and the single-chip receiver. The AWESOME receiver data is on the left and the single-chip receiver data is on the right. Each spectrogram shows eight seconds of data and was taken using the same north-south antenna at the Packard Electrical Engineering building. It is important to point out that the gain of the two receivers is not the same. This was corrected by shifting the AWESOME data to compensate for this difference.

The two data samples were taken approximately 10 minutes apart, so the spectrograms are not expected to be identical. However, given the small time differential, it is expected that the same transmitters will be visible and the same interfering signals will be present in both samples. The data collected is consistent with these expectations. Aside from differences in the sferics and the high frequency roll-off of the AWESOME receiver, it is difficult to discern any significant difference between

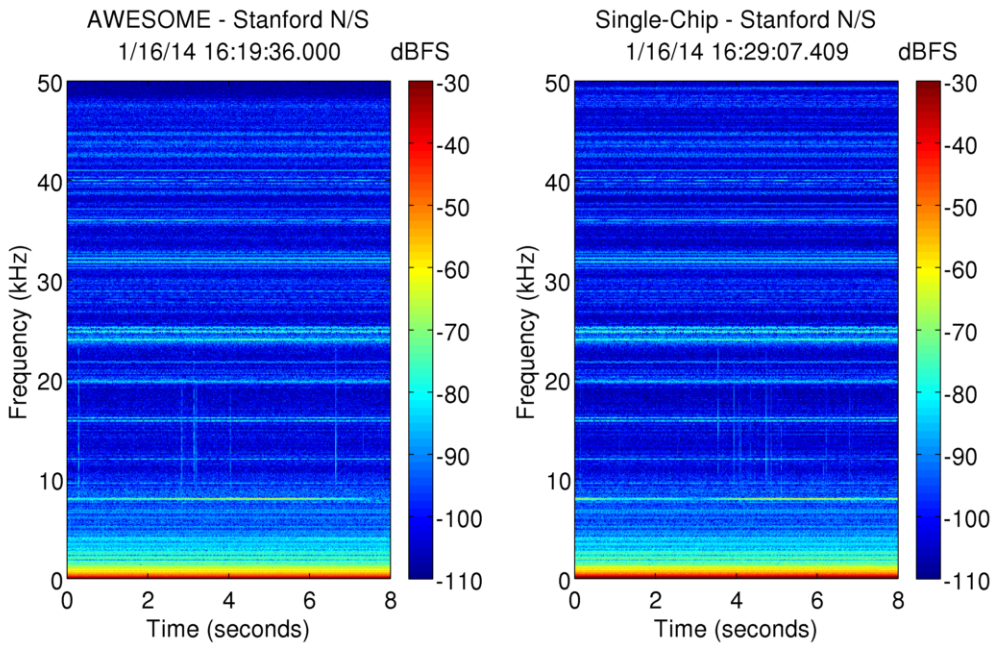


Figure 5.42: Side-by-side comparison of data collected at Stanford University with the AWESOME receiver (left) and the single-chip receiver (right).

the two spectrograms.

The average spectrum was calculated to more accurately compare the two data samples. This was accomplished by taking the average at each frequency over the full eight seconds of data. Using this method a small random variation, such as a sferic, won't significantly affect the result due to the large number of data points in the sample. The average spectrum for each receiver is shown in Figure 5.43. The horizontal axis represents frequency and the vertical axis represents the average signal strength. The AWESOME receiver data is the blue curve and the single-chip receiver data is the red curve.

There is good agreement between the two data samples. All of the same transmitters are present with similar amplitudes and the interference also matches well. The most noticeable difference is at frequencies above approximately 47 kHz. Above this frequency the AWESOME data is suppressed. This is due to the roll-off of the anti-alias filter in the AWESOME receiver. Although it is difficult to tell from the plot, it also appears that the single-chip receiver has a slightly lower noise floor than

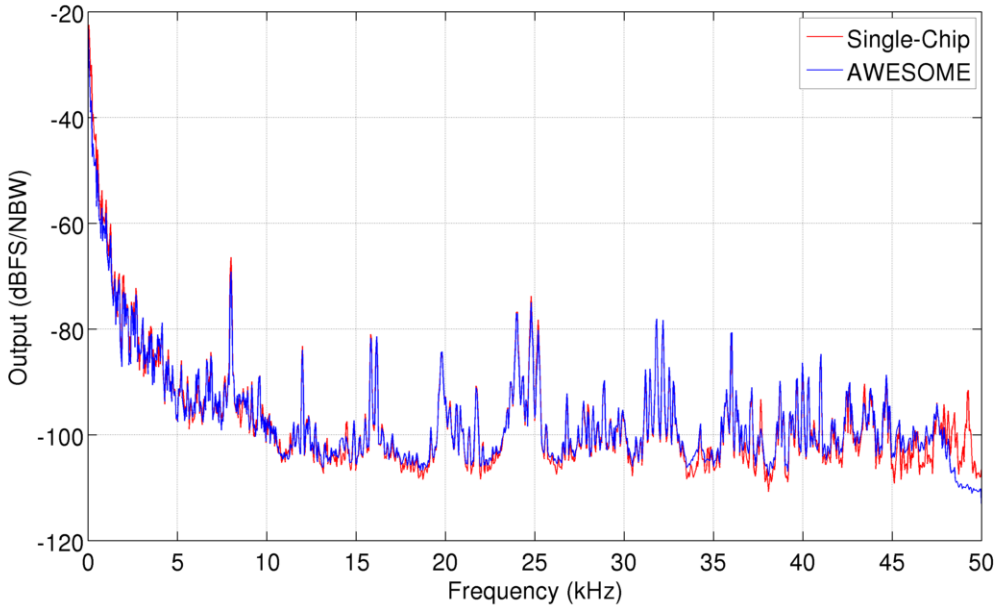


Figure 5.43: Comparison of the average spectrum.

the AWESOME receiver.

One metric that is often used to compare VLF receiver performance is to look at the signal-to-noise ratio of the spectrum around a strong transmitter. The NLK and NML transmitters can be used for this purpose. Figure 5.44 shows the average spectrum of the data zoomed in on the frequency range from 22 kHz to 28 kHz.

Both transmitters are clearly visible when zooming in on the average spectrum. NLK is at 24.8 kHz and NML is at 25.2 kHz. A third transmitter is visible at 24 kHz, which is the NAA transmitter in Cutler, Maine. The strength of the transmitters is not exactly equal in the two data samples, but since the data was taken approximately 10 minutes apart this is not unexpected as the propagation conditions change over time. However, what is important is the lower noise floor in the spectrum of the single-chip receiver. The lower noise floor results in a larger signal-to-noise ratio. As a result, in this side-by-side comparison the single-chip receiver outperforms the AWESOME receiver.

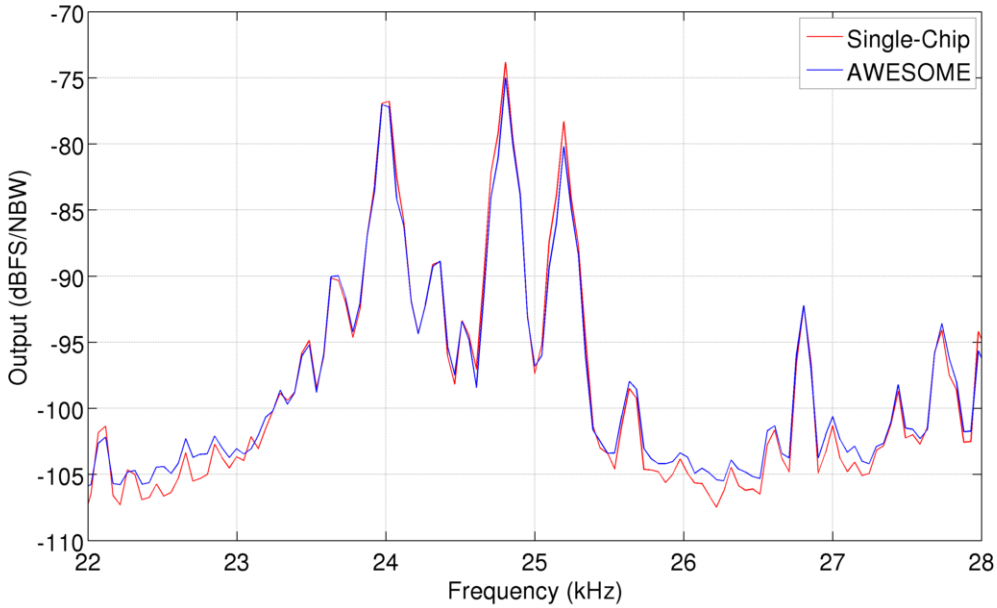


Figure 5.44: Comparison of the average spectrum zoomed in around the NLK and NML transmitters.

Chapter 6

Conclusion

This dissertation covered the design, implementation and validation of the first single-chip broadband VLF magnetic field receiver. The single-chip receiver implements the full signal path of a traditional VLF receiver, which includes interfacing with the 1 Ω, 1 mH loop antenna, processing the received signal and generating digital output data. To achieve this functionality, the single-chip receiver includes a low-impedance low-noise amplifier and a continuous-time delta-sigma analog-to-digital converter.

The low-noise amplifier was implemented with a two-stage architecture. The first stage consists of a low-impedance common-base amplifier, which uses NPN transistors to achieve good $1/f$ noise performance. The second stage uses a differential instrumentation amplifier that employs high gain OTAs and feedback to ensure minimal harmonic distortion. The LNA has four gain modes that enable the performance of the receiver to be optimized based on the requirements of the application. This LNA is the first integrated VLF magnetic field low-noise amplifier to simultaneously achieve better than 1 $\mathrm{fT/Hz^{1/2}}$ sensitivity and over 90 dB spurious-free dynamic range, which is a result that was thought to be unlikely to be achieved just a few years ago [32]. The LNA also demonstrates the use of an automatic biasing system that increases the robustness of the receiver to variations in temperature. The LNA consumes approximately 908 µW.

The analog-to-digital converter was implemented with a continuous-time delta-sigma modulator. The delta-sigma ADC architecture combines oversampling and

noise shaping to create a high resolution ADC from lower resolution components. The delta-sigma architecture is relatively immune to mismatch and other non-ideal effects. The primary reason for selecting this ADC architecture was that the continuous-time loop filter provides a free anti-alias filter, which leads to a significant power savings. The ADC uses a clock frequency of 15 MHz, which corresponds to an oversampling ratio of 150. It achieves a resolution of 12.40 bits and a spurious-free dynamic range of 93.60 dB. The power dissipation of the ADC is roughly 640 µW.

The single-chip receiver was fabricated in a 0.13 µm BiCMOS process. It has a total power consumption of approximately 1.55 mW and uses a 1.2 V supply voltage. This power dissipation corresponds to a reduction of over 30 times compared to the signal path power consumption of the Penguin receiver, which is the current low-power VLF receiver. In addition to measuring the receiver performance in the lab, the receiver was also tested in the field at Stanford University and at a quiet site in the Santa Cruz Mountains. The field test demonstrated that the data quality of the single-chip receiver was just as good, if not better, than that of the AWESOME receiver, which is the current high performance VLF receiver deployed by the Stanford VLF research group.

6.1 Future Work

The successful implementation of the single-chip VLF magnetic field receiver opens up several possibilities for further research. The research ideas can be divided into two categories: improvements to the receiver and applications for the receiver.

In terms of improving the receiver, one attractive idea would be to implement the entire receiver in CMOS to take advantage of the advanced short-channel CMOS processes that are currently available. The reason this was not done in the current design was because CMOS devices typically have inferior $1/f$ noise performance. As a result, bipolar transistors were used in the input stage of the LNA to meet the noise requirements. There are several strategies that could be employed to overcome the $1/f$ noise disadvantage of CMOS transistors. One method of particular interest is chopping, which would not only solve the $1/f$ noise problem, but would also have the

added benefit of canceling any offset in the LNA [21].

There are also several possibilities for further work at the system-level of the receiver. One possible improvement would be to implement an automatic gain control system, which automatically changes the gain of the LNA depending on the characteristics of the received signal. For example, if large interfering signals are detected, the system would reduce the gain to prevent the receiver from clipping. Another idea would be to automatically scale the power dissipation of the receiver depending on the noise and dynamic range requirements. In many cases, the full dynamic range of the receiver is not required and the power dissipation could be reduced. This optimization could significantly increase the battery life of a remotely deployed receiver.

While the single-chip receiver implements the full signal path functionality of a VLF magnetic field receiver, further work would be needed to build a complete receiver system based on the single-chip receiver. In addition to the signal path, a full receiver would need to add a time-reference, clock generator, digital signal processing, data storage and power management. This could be accomplished using separate components to implement these functions, or the receiver could be further optimized by integrating some of this functionality on-chip.

There are many possible applications for the single-chip receiver. Due to its small size, one idea of particular interest would be to build a hand-held VLF receiver. This hand-held receiver could be used to survey locations to find quiet sites where large permanent antennas could be constructed. It could also be used more widely as a method to detect and monitor power-line interference. The implementation of a hand-held receiver would require further innovation to reduce the size of the antenna and input transformer, as both of these components are currently much too large for a hand-held device.

The Stanford VLF research group has deployed a number of satellite-based instruments. Future work on the single-chip receiver could include hardening the receiver to the effects of radiation, which is encountered in space. This could be accomplished by redesigning the circuits using radiation-hard techniques, or by appropriately shielding the chip. The single-chip receiver would be particularly well suited for a satellite-based application, because size is often a significant constraint.

Bibliography

[1] Andrew Alford and A. G. Kandoian. Ultrahigh-frequency loop antennas. *AIEE Transactions*, 59(12):843–848, Feb 1940.

[2] Rex T. Baird and Terri S. Fiez. Improved $\Delta\Sigma$ DAC linearity using data weighted averaging. *IEEE International Symposium on Circuits and Systems*, 1:13–16, May 1995.

[3] Philippe Benabes, Mansour Keramat, and Richard Kielbasa. A methodology for designing continuous-time sigma-delta modulators. *Proceedings of the European Design and Test Conference*, pages 46–50, Mar 1997.

[4] Brian P. Brandt, Drew E. Wingard, and Bruce A. Wooley. Second-order sigma-delta modulation for digital-audio signal acquisition. *IEEE Journal of Solid-State Circuits*, 26(4):618–627, Apr 1991.

[5] Lucian J. Breems, Eric J. van der Zwan, and Johan H. Huijsing. Design for optimum performance-to-power ratio of a continuous-time $\Sigma\Delta$ modulator. *Proceedings of the European Solid-State Circuits Conference*, pages 318–321, Sep 1999.

[6] Emmanuel J. Candès and Michael B. Wakin. An introduction to compressive sampling. *IEEE Signal Processing Magazine*, 25(2):21–30, Mar 2008.

[7] James C. Candy. Decimation for sigma delta modulation. *IEEE Transactions on Communications*, COM-34(1):72–76, Jan 1986.

[8] L. Richard Carley. A noise-shaping coder topology for 15+ bit converters. *IEEE Journal of Solid-State Circuits*, 24(2):267–273, Apr 1989.

[9] Bruce Carter. A differential op-amp circuit collection. Application report, Texas Instruments, Dallas, TX, Jul 2001. SLOA064.

[10] Kirk C.-H. Chao, Shujaat Nadeem, Wai L. Lee, and Charles G. Sodini. A higher order topology for interpolative modulators for oversampling A/D converters. *IEEE Transactions on Circuits and Systems*, 37(3):309–318, Mar 1990.

[11] David K. Cheng. *Fundamentals of Engineering Electromagnetics*. Prentice-Hall, 1993.

[12] James A. Cherry and W. Martin Snelgrove. Clock jitter and quantizer metastability in continuous-time delta-sigma modulators. *IEEE Transactions on Circuits and Systems II*, 46(6):661–676, Jun 1999.

[13] James A. Cherry and W. Martin Snelgrove. *Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion*. Kluwer, 1999.

[14] James A. Cherry and W. Martin Snelgrove. Excess loop delay in continuous-time delta-sigma modulators. *IEEE Transactions on Circuits and Systems II*, 46(4):376–389, Apr 1999.

[15] D. A. Chrissan and A. C. Fraser-Smith. Seasonal variations of globally measured ELF/VLF radio noise. *Radio Science*, 31(5):1141–1152, Sep-Oct 1996.

[16] Hugh J. Christian, Richard J. Blakeslee, Dennis J. Boccippio, William L. Boeck, Dennis E. Buechler, Kevin T. Driscoll, Steven J. Goodman, John M. Hall, William J. Koshak, Douglas M. Mach, and Michael F. Stewart. Global frequency and distribution of lightning as observed from space by the optical transient detector. *Journal of Geophysical Research*, 108(D1), Jan 2003.

[17] Morris B. Cohen. *ELF/VLF Phased Array Generation via Frequency-Matched Steering of a Continuous HF Ionospheric Heating Beam*. Ph.D. Dissertation, Stanford University, Oct 2009.

[18] Morris B. Cohen. The Stanford University ELF/VLF receiver: Narrowband transmitter guide. Technical report, Stanford University, Stanford, CA, Jul 2009.

[19] Morris B. Cohen, Umran S. Inan, and Evans W. Pascal. Sensitive broadband ELF/VLF radio reception with the AWESOME instrument. *IEEE Transactions on Geoscience and Remote Sensing*, 48(1):3–17, Jan 2010.

[20] Kenneth Davies. *Ionospheric Radio Propagation*. National Bureau of Standards, 1965.

[21] Christian C. Enz and Gabor C. Temes. Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization. *Proceedings of the IEEE*, 84(11):1584–1614, Nov 1996.

[22] H. T. Friis. Noise figures of radio receivers. *Proceedings of the IRE*, 32(7):419–422, Jul 1944.

[23] Ranjit Gharpurey and Robert G. Meyer. Modeling and analysis of substrate coupling in integrated circuits. *IEEE Journal of Solid-State Circuits*, 31(3):344–352, Mar 1996.

[24] K. L. Graf, M. Spasojevic, R. A. Marshall, N. G. Lehtinen, F. R. Foust, and U. S. Inan. Extended lateral heating of the nighttime ionosphere by ground-based VLF transmitters. *Journal of Geophysical Research: Space Physics*, 118:7783–7797, Dec 2013.

[25] Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, and Robert G. Meyer. *Analysis and Design of Analog Integrated Circuits*. Wiley, 5th edition, 2009.

[26] Roubik Gregorian, Kenneth W. Martin, and Gabor C. Temes. Switched-capacitor circuit design. *Proceedings of the IEEE*, 71(8):941–966, Aug 1983.

[27] Mikael Gustavsson, J. Jacob Wikner, and Nianxiong Nick Tan. *CMOS Data Converters for Communications*. Kluwer, 2000.

[28] Sarah K. Harriman. *Custom Integrated Amplifier Chip for VLF Magnetic Receiver*. Ph.D. Dissertation, Stanford University, Aug 2010.

[29] Alan Hastings. *The Art of Analog Layout*. Pearson, 2nd edition, 2006.

[30] Robert A. Helliwell. *Whistlers and Related Ionospheric Phenomena*. Stanford, 1965.

[31] Maxim Integrated. Dynamic testing of high-speed ADCs, part 2. Application note, San Jose, CA, Jul 2002. APP 729.

[32] Max Klein. *Autonomous Ultra-Low Power ELF/VLF Receiver Systems*. Ph.D. Dissertation, Stanford University, Nov 2009.

[33] Takayuki Konishi, Kenji Inazu, Jun Gyu Lee, Masanori Natsui, Shoichi Masui, and Boris Murmann. Design optimization of high-speed and low-power operational transconductance amplifier using g_m/I_D lookup table methodology. *IEICE Transactions*, E94-C(3):334–345, Mar 2011.

[34] Thomas H. Lee. *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, 2nd edition, 2004.

[35] J. D. Li, M. Spasojevic, V. Harid, M. B. Cohen, M. Golkowski, and U. Inan. Analysis of magnetospheric ELF/VLF wave amplification from the siple transmitter experiment. *Journal of Geophysical Research: Space Physics*, 119:1837–1850, Mar 2014.

[36] Robert Andrew Marshall. *Very Low Frequency Radio Signatures of Transient Luminous Events Above Thunderstorms*. Ph.D. Dissertation, Stanford University, May 2009.

[37] Benjamin Joseph Mossawir. *High-Fidelity, Broadband Amplification and Filtering for Spaceborne Instrumentation*. Ph.D. Dissertation, Stanford University, December 2009.

[38] M. Ortmanns and F. Gerfers. *Continuous-Time Sigma-Delta A/D Conversion*. Springer, 2006.

[39] Evans W. Paschal. The design of broad-band VLF receivers with air-core loop antennas. Technical report, Stanford University, Stanford, CA, May 1988.

[40] Donald O. Pederson and Kartikeya Mayaram. *Analog Integrated Circuits for Communication*. Springer, 2nd edition, 2008.

[41] Marcel J. M. Pelgrom, AAD C. J. Duinmaijer, and Anton P. G. Welbers. Matching properties of MOS transistors. *IEEE Journal of Solid-State Circuits*, 24(5):1433–1440, Oct 1989.

[42] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. McGraw-Hill, 2001.

[43] R. K. Said, U. S. Inan, and K. L. Cummins. Long-range lightning geolocation using a VLF radio atmospheric waveform bank. *Journal of Geophysical Research*, 115:D23108, Dec 2010.

[44] Richard Schreier. Delta Sigma Toolbox for MATLAB. `http://www.mathworks.com/matlabcentral/fileexchange/`, Jan 2000.

[45] Richard Schreier and Gabor C. Temes. *Understanding Delta-Sigma Data Converters*. Wiley, 2005.

[46] David K. Su, Marc J. Loinaz, Shoichi Masui, and Bruce A. Wooley. Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits. *IEEE Journal of Solid-State Circuits*, 28(4):420–430, Apr 1993.

[47] Kevin E. Trenberth and Jerry G. Olson. Temperature trends at the South Pole and McMurdo Sound. *Journal of Climate*, 2:1196–1206, Oct 1989.

[48] Martin A. Uman. *The Lightning Discharge*. Academic Press, 1987.

[49] Charles Chang-I Wang. *High Fidelity Analog-to-Digital Conversion for Spaceborne Applications*. Ph.D. Dissertation, Stanford University, Sep 2009.

[50] Bo Xia, Shouli Yan, and Edgar Sánchez-Sinencio. An RC time constant autotuning structure for high linearity continuous-time $\Sigma\Delta$ modulators and active filters. *IEEE Transactions on Circuits and Systems*, 51(11):2179–2188, Nov 2004.

[51] Shouli Yan and Edgar Sánchez-Sinencio. Low voltage analog circuit design techniques: A tutorial. *IEICE Transactions on Analog Integrated Circuits and Systems*, E00-A(2):1–17, Feb 2000.

[52] J. Yuan and C. Svensson. New single-clock CMOS latches and flipflops with improved speed and power savings. *IEEE Journal of Solid-State Circuits*, 32(1):62–69, Jan 1997.

[53] F. G. Zoghzoghy, M. B. Cohen, R. K. Said, and U. S. Inan. Statistical patterns in the location of natural lightning. *Journal of Geophysical Research: Atmospheres*, 118:787–796, Jan 2013.